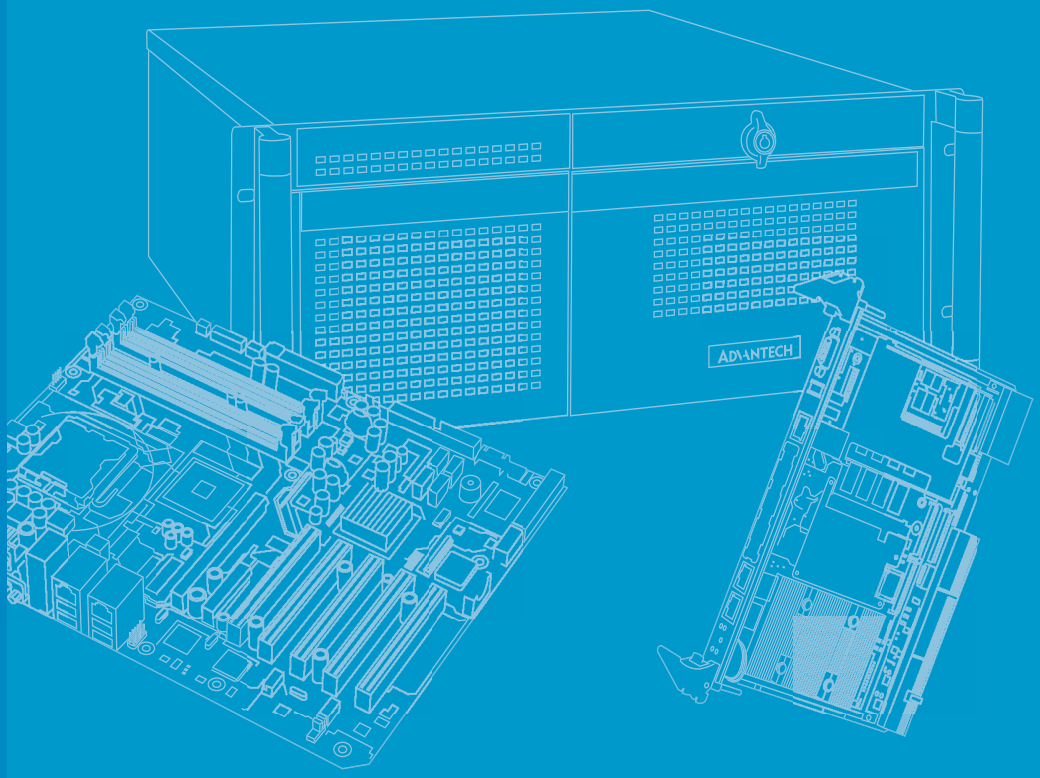

User Manual

MIC-6314

OpenVPX 6U CPU Blade with 4th/5th Gen Intel® Xeon® E3v4/ Core™ Processor

ADVANTECH

Enabling an Intelligent Planet

Copyright

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Product Warranty (2 years)

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Please consult your dealer for more details.

If you think your product is defective, follow the steps below.

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any messages displayed onscreen when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any relevant information readily available.
3. If your product is diagnosed as defective, obtain a return merchandize authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a completed Repair and Replacement Order card and a proof of purchase date (such as a photocopy of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
5. Write the RMA number clearly on the outside of the package and ship the product prepaid to your dealer.

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Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This type of cable is available from Advantech. Please contact your local supplier for ordering information.

FCC Class A

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference. In such cases, users are required to correct the interference at their own expense.

FM

This equipment has passed the FM certification. According to the National Fire Protection Association, work sites are classified into different classes, divisions, and groups based on hazard considerations. This equipment is compliant with the specifications for Class I, Division 2, Groups A, B, C, and D indoor hazards.

Technical Support and Assistance

1. Visit the Advantech website at http://support.advantech.com to obtain the latest product information.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before calling:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Warnings, Cautions, and Notes

Warning! *Warnings indicate conditions that if not observed can cause personal injury!*

Caution! *Cautions are included to help prevent hardware damage or data losses.*

For example,

"Batteries are at risk of exploding if incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions."

Note! *Notes provide additional optional information.*

Document Feedback

To assist us in making improvements to this manual, we welcome any comments and constructive criticism. Please send all comments in writing to support@advantech.com

Packing List

Before setting up the system, check that the items listed below are included in the shipment and in good condition. If any item is missing or damaged, please contact your dealer immediately.

- 1 x MIC-6314 all-in-one single board computer (CPU heatsink and PCH heatsink included)
- 1 x storage carrier (2.5" hard drive/ SSD, or M.2) (assembled)
- 1 x Solder side cover (assembled)
- 1 x RJ45 to DB9 cable
- 1 x Warranty certificate
- Safety Warnings: CE, FCC class A

Safety Instructions

1. Read these safety instructions carefully.
2. Retain this user manual for future reference.
3. Disconnect this equipment from all AC outlets before cleaning. Use only a damp cloth for cleaning. Do not use liquid or spray detergents.
4. For plugable equipment, the power outlet socket must be located near the equipment and easily accessible.
5. Protect this equipment from humidity.
6. Place the equipment on a reliable surface during installation. Dropping or letting the equipment fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. Do not cover the openings.
8. Ensure that the voltage of the power source is correct before connecting the equipment to the power outlet.
9. Position the power cord away from high-traffic areas. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage from transient overvoltage.
12. Never pour liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If one of the following occurs, have the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated into the equipment.
    - The equipment has been exposed to moisture.
    - The equipment does not work well, or you cannot get it to work according to the user's manual.
    - The equipment has been dropped and damaged.
    - The equipment has obvious signs of breakage.
15. Do not leave this equipment in an environment where the storage temperature fluctuates below -55 °C (-67 °F) or above 105 °C (221 °F) as this may cause damage. The equipment should be stored in a controlled environment.
16. Batteries are at risk of exploding if incorrectly replaced. Replace only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer’s instructions.

The sound pressure level at the operator's position does not exceed 70 dB (A) in accordance with the IEC 704-1:1982 specifications.

DISCLAIMER: These instructions are provided according to the IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from the PC chassis before manual handling. Do not touch any components on the CPU card or other cards while the PC is powered on.
- Disconnect the power before making any configuration changes. The sudden rush of power as a jumper is connected or a card installed may damage sensitive electronic components.

We Appreciate Your Input

Please let us know if any aspect of this product, including the manual, could benefit from improvements or corrections. We appreciate your valuable input in helping make our products better.

Contents

Chapter 1

Hardware Configuration

This chapter explains how to configure the MIC-6314 hardware.

1.1 Introduction

The MIC-6314 is Advantech's next generation single processor 6U VPX blade, based on the 4th/ 5th Generation Intel® Core™ embedded platform with increased cache size and efficiency, as well as instruction set improvements. The MIC-6314 provides two configurable PCIE x 8 ports in the VPX data plane and two PCI Express ports x8 lanes in the VPX expansion plane to enable the highest performance available in the 6U VPX form factor compute intense applications. These PCIE interfaces offer high speed up to PCIE gen. 2 (5Gb/s) throughput, low latency, scalable, error recoverable deterministic inter connectivity to the mainstream peripherals and I/O cards such as DSP and FPGA cards. The PCIE widths and ports on the data plane and the extension plane of MIC-6314 is user configurable, which make MIC-6314 capable to replace the PCIE switch blade in a small system.

With a SO-DIMM socket and additional soldered, onboard DRAM with ECC in a dual channel design running up to 1600MT/s, the MIC-6314 can be integrated into various harsh environments while maintaining maximum memory throughput, and supports memory expansion by using the latest SO-DIMM technology simultaneously.

Tailored for harsh environments, the MIC-6314 has a native ruggedized convection cooled heat sink adaptable to various chassis environments; with the alternated optional air cooled heat sink, additional I/O is provided on the front panel. An onboard soldered, industrial SSD is included for maximum reliability, and a SSD socket is also available for a cost-efficient, modular storage. By using Intel®'s powerful PCH (Lynx Point) with its advanced SATA controller, the MIC-6314 offers high storage capacity at up to 6Gbps transfer speed. An onboard XMC site with PCIe x8 gen.3 connectivity can host high speed offload or I/O mezzanines. Two USB 3.0 ports on the front panel can connect to external devices with up to 5Gbps data rate. Network and remote connectivity can be achieved via a RS-232 console (RJ-45) and two GbE RJ-45 ports, powered by Intel®'s latest Gigabit Ethernet controller.

The Intel® next generation graphics engine Iris Pro offers up to 2x the graphic performance compared to previous generation solutions. Triple independent display support can be implemented by using VGA and 2 DVI ports on MIC6314. Audio is powered by a ALC892 controller via the backplane interface, and provides media support. A PCIE interface is reserved for the optional M.2 high speed storage.Besides the modern M.2 storage, three SATA III one SATA II and seven USB ports (2x USB 3.0, 5x USB 2.0) are also connected to the backplane to fulfill the demand for extra IO ports or storage. Four GbE ports (two SERDES selectable) support system level IP connectivity, and four UART interfaces (RS232/422/485 selectable) can be leveraged to interface to legacy devices and consoles.

1.1.1 MIC-6314 SKU introduction

Table 1.1: Processor Type

MIC-6314 Model Number	CPU	Number of Cores	Cooling Method	External Storage (not included)	XMC
MIC-6314-A1A4E	I7-5850EQ	4	Convection cooling	SSD	--
MIC-6314-A2A4E	I7-5850EQ	4	Convection cooling	PCIE M.2	Yes
MIC-6314-B1C4E	i5-4402E	2	Ruggedized convection cooling	SSD	--

1.2 Specifications

1.2.1 OpenVPX Interface

MIC-6314 is compliant with the OpenVPX MOD6-PAY-4F1Q2U2T-12.2.1-2 profile. Two lanes of PCEI x 8 are provided in the P1 dataplane. Another two lanes of PCIe x8 are routed to the P2 expansion plane. All of these PCIE lanes come from a gen. 3 PCIE switch respectively. Please contact the Advantech representatives for the different configuration availability. Two lanes of 1GBase-T (can be configured to SerDes upon request) are employed for the P4 control plane. Another two lanes of 1GBase-T are routed to the P6 user define plane.

1.2.2 CPU

MIC-6314 supports Intel® Xeon® E3Lv4 and Core™ i5-4402E processors, with clock frequencies of up to 3.4 GHz. The Intel® Xeon® E3Lv4 processor is integrated with the Intel® Iris™ Pro Graphics P6300 embedded graphics controller that supports OpenGL 4.3, DirectX 11.2, and OpenCL 2.0 for enhanced 3D graphics processing. Moreover, the Intel® Xeon® E3Lv4 processor is equipped with Intel® Turbo Boost Technology 2.0, which activates automatically when the OS requests the highest processor performance state.

Meanwhile, the 4th Gen Intel® Core™ i5-4402E processor offers a two-fold improvement in performance compared to that of the previous generation. Finally, the inclusion of Intel® HT Technology enables MIC-6314 to execute multiple demanding applications simultaneously, while maintaining system responsiveness.

1.2.3 Processor

The Intel® i7-5850EQ processor is the default for the air-cooled MIC-6314 SKU (MIC-6314-A series with i7-5850EQ), whereas the Intel® Core™ i5-4402E processor is the default for the conduction-cooled MIC-6314 SKU (MIC-6314-B series).

Please contact your distributor or local Advantech representative for information regarding the availability of other Xeon® E3Lv4 or 4th/5th Gen Core™ SKUs.

Table 1.2: Processor Type

Intel CPU Model Number	CPU architecture	# cores	Graphic Engine	Freq.	Cache	DMI	CPU TDP
i7-5850EQ	Broadwell (14nm)	4	Intel® Iris™ Pro Graphics P6200	3.4GHz (max)	6MB	5 GT/s	47W
i5-4402E	Haswell (22nm)	2	Intel® HD Graphics 4600	2.7 GHz	3 MB	5 GT/s	25W

Note! *Because power consumption and thermal restrictions vary between different VPX systems, please double check these items before installing a higher speed CPU not specified in the table above.*

1.2.4 BIOS

MIC-6314 features an 8 Mbyte SPI flash containing a board-specific BIOS (from AMI) designed to meet industrial and embedded system requirements.

1.2.5 Chipset

The Intel® Mobile QM87 (Lynx Point) chipset integrates several capabilities to provide flexibility for connecting I/O devices. The Intel® QM87 chipset offers fast access to peripheral devices and delivers outstanding performance through high bandwidth interfaces, such as PCI Express, Serial ATA, and integrated USB 3.0. The chipset also reduces power consumption through the enhanced link power management of the Advanced Host Controller Interface (AHCI), enables easy expansion with native hot plug support, and enhances boot and multi-tasking performance with native command queuing (NCQ).

1.2.6 Memory

MIC-6314 is equipped with 8 GB of onboard DDR3L memory with ECC support. The SKU with convection heatsink also has one 204-pin SODIMM socket that can accommodate an additional 8GB of 1.35V memory.

The following SODIMMs have been verified with this product:

Brand	Size	Speed	Vendor PN	ECC	Pin Count	Memory Chip
ATP	8 GB	DDR3L 1600	AW24P7228BLK0M	Yes	204 pins	Micron
Advantech	8 GB	DDR3L 1600	AQD-SD3L8GE16-SG	Yes	204 pins	Samsung
	8 GB	DDR3L 1600	AQD-SD3L8GE16-MG	Yes	204 pins	Micron

1.2.7 Ethernet

MIC-6314 features two Intel® I210 LAN controllers to provide two lanes of 10/100/1000Base-T Ethernet connectivity (on LAN 1 and 2) to the front panel, while four 10/100/1000Base-T Ethernet lanes are provided to P4 and P6 with I350AM4.

- Front I/O (RJ45)
- Backplane

To configure the two P4 lanes of Ethernet to SerDes, contact your local Advantech representative for assistance.

1.2.8 Storage Interface

The MIC-6314 supports four ports of SATA III and two SATA II interfaces. A SATA III interface is routed to the SATA connector on the daughter board. The rest of three SATAIII are routed to P5. Two SATA II interfaces are connected to an onboard soldered, industrial SSD for maximum reliability and the backplane via P5 respectively. The default onboard flash capacity is 64GB. For different onboard flash capacity, please contact your local Advantech branch or distributor to offer the customized option.

MIC-6314 also provides a M.2 daughter board in the MIC-6314-A2A4E SKU. This M.2 has a PCIe gen. 2 x 2 interface, and it supports PCIe M-key type M.2 therefore.

1.2.9 Serial Ports

MIC-6314 supports 4 COM ports. COM1 and COM2 are switchable to the onboard RJ45 COM port or RTM. All COM ports can be configured to RS232/RS422/RS485 mode via the onboard switch.

1.2.10 USB Ports

Two USB 3.0 compliant ports with fuse protection are provided. Both ports are routed to the front panel connectors on MIC-6314. Two additional USB 3.0 ports are routed to the rear I/O module via the P5 connector. Besides USB 3.0 ports, one USB 2.0 port is provided to the front panel (the air cooled SKU), and another five ports to the backplane P6.

1.2.11 LEDs

Four LEDs are provided on the front panel as follows:

- One blue LED indicates hot-swap capability. The blue color indicates that the board can be safely removed from the system.
- One yellow LED indicates HDD status. A blinking light indicates HDD activity.
- One LED indicates power status. When the LED light is green, power is being provided to the board.
- One LED indicates BMC status. The light is green when the BMC is present.

1.2.12 Watchdog Timer

An onboard watchdog timer provides system reset capabilities via software control.

The programmable time intervals range from 1 to 255 seconds. This function is enabled by default in the SKU with IPMI management. Should you require this function in the SKU without IPMI management, please contact your local field service engineer or salesperson.

1.2.13 Optional Rear I/O Modules

Please contact your local Advantech representative or distributor for custom RI/O inquires.

1.2.14 Mechanical and Environmental Specifications

- **Operating Temperature:** -40 ~ 70 °C (32 ~ 131 °F)

Note! *The MIC-6314's operating temperature range depends on the processor installed and the airflow through the chassis.*

- **Storage Temperature:** -40 ~ 85 °C (-40 ~ 185 °F)
- **Humidity:** 95% @ 40 °C (non-condensing)
- **Humidity (Non-Operating):** 95% @ 60 °C (non-condensing)
- **Vibration:** VITA47, V2 (conduction cooled SKU with onboard flash only) 0.008 g²/Hz, 2 Grms, 5-500Hz (convection cooled)
- **Shock:** 40G (with onboard flash only)
- **Altitude:** 50,000 m above sea level
- **Board Size:** 233.35 x 160 mm (6U size), 1-slot (4 TE) wide
- **Weight:** 0.95 kg

1.2.15 Compact Mechanical Design

The MIC-6314's mechanical design is compliant with VITA 48.2, REDI specifications. The MIC-6314-B1C4E model is Advantech's standard conduction-cooled SKU. For custom conduction-cooled heatsink designs, please check with your distributor or local Advantech representative for feasibility.

1.2.16 PCIE Bridge

MIC-6314 uses a PLX PEX8733 component, a 32-lane, 8-port, Gen 3 PCIe switch device as a gateway for intelligent subsystems. When configured as a system controller, the bridge acts as a standard transparent PCI Express bridge. MIC-6314 receives power from the backplane and supports rear I/O. The PLX PEX8733 component offers the following features:

- PCIe interface:
  - PCI Express Base Specification, r3.0
- Supports transparent and non-transparent operation modes
- Supports forward and reverse bridging
- End-to-end CRC (ECRC) and Poison bit support
- Failover support, can be configured for 1+1 redundancy or N+1 redundancy

Please consult the PLX PEX8733 data book for details.

1.2.17 I/O Connectivity

The MIC-6314's front panel I/O is provided by two RJ45 Gigabit Ethernet ports, one RJ45 COM port, two USB 3.0 ports, one USB 2.0, one DVI connector, and one XMC/PMC knockout.

	Front Panel				Main On-board Features	
Part Number	Display	USB	Ethernet (RJ45)	Console (RJ45)	CPU	SODIMM Socket
MIC-6314-A1A4E	DVI x1	2.0x1; 3.0x2	2	1	I7-5850EQ	Yes
MIC-6314-A2A4E	DVI x1	2.0x1; 3.0x2	2	1	I7-5850EQ	Yes
MIC-6314-B1C4E	VGA x1	3.0x2	0	0	i5-4402E	No

The onboard I/O consists of one SATA channel that can be connected to a daughter board or a CFast slot. Rear I/O connectivity is available via the following VPX connectors:

- P1: Two PCIe x8
- P2: Two PCIe x8
- P4: XMC I/O, GPIO, two lanes of GbE or SerDes
- P5: Four SATA ports (3 SATA III ports and one SATA II port), two COM ports, two DVI ports, two USB 2.0, and two USB 3.0
- P6: Two GbE, five USB 2.0, keyboard/mouse, two COM ports, Line-In, Line-Out, and Mic

Please refer to the appendix for detailed pin definitions.

1.2.18 XMC (Switched Mezzanine Card) VITA 42 Compliant

Additional I/O or co-processing functionality is supported by add-on PMC modules. MIC-6314 supports one XMC site that is fully compliant with the VITA 46.9 PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard specification.

The two-layer front panel design complies with IEEE 1101.10. All connectors are firmly screwed to the front panel, and a shielding gasket is attached to the panel edge, reducing emissions and increasing protection from external interference.

1.2.19 Hardware Monitor

A hardware monitor (NCT7904D) is available for monitoring critical hardware parameters. The monitor is attached to the BMC for monitoring the CPU temperature and core voltage.

1.2.20 Super I/O

The MIC-6314 Super I/O device supports the following legacy PC devices:

- Four serial ports connected to the rear I/O module (COM1 to COM4) or front panel via a multiplexer in the FPGA (COM1 or COM2).
- The PS2 (keyboard/mouse) is routed to the rear I/O module.

1.2.21 RTC and Battery

The RTC module maintains the date and time. On the MIC-6314 model, the RTC circuitry is connected to battery sources (CR2032M1S8-LF, 3V, 210mAH).

1.2.22 IPMI

MIC-6314 uses the Intelligent Platform Management Interface (IPMI) to monitor the system health. A NXP LPC1768 microcontroller provides BMC functionality to interface between the system management software and platform hardware. Full IPMI details are provided in Chapter 3.

1.2.23 BMC

The management firmware of MIC-6314 is implemented on a 32-bit ARM Cortex-M3 core. An external SPI EEPROM is used for storing field-replaceable unit (FRU) inventory data and non-volatile configurations.

1.2.23.1 Key Features

- Advantech integrity sensor
- Based on Advantech's IPMI core and designed for xTCA, CPCI, and VPX
- Compliant with IPMI 1.5 and IPMI 2.0 specifications
- IPMI-over-LAN
- Serial-over-LAN
- KCS interface for direct IPMI communication between the operating system and BMC
- BIOS fail over, including BIOS watchdog
- Full BMC Watchdog support as defined in the IPMI specification
- Full BMC firmware redundancy
  - Manual roll back
  - Automatic roll back for update failure
- HPM.1 for in field updates, supporting
  - BMC firmware
  - FPGA
  - BIOS
- UART muxing between all serial interfaces for easy console access (UART1, UART2 only)
- Additional sensors for hardware monitoring

1.3 Functional Block Diagram

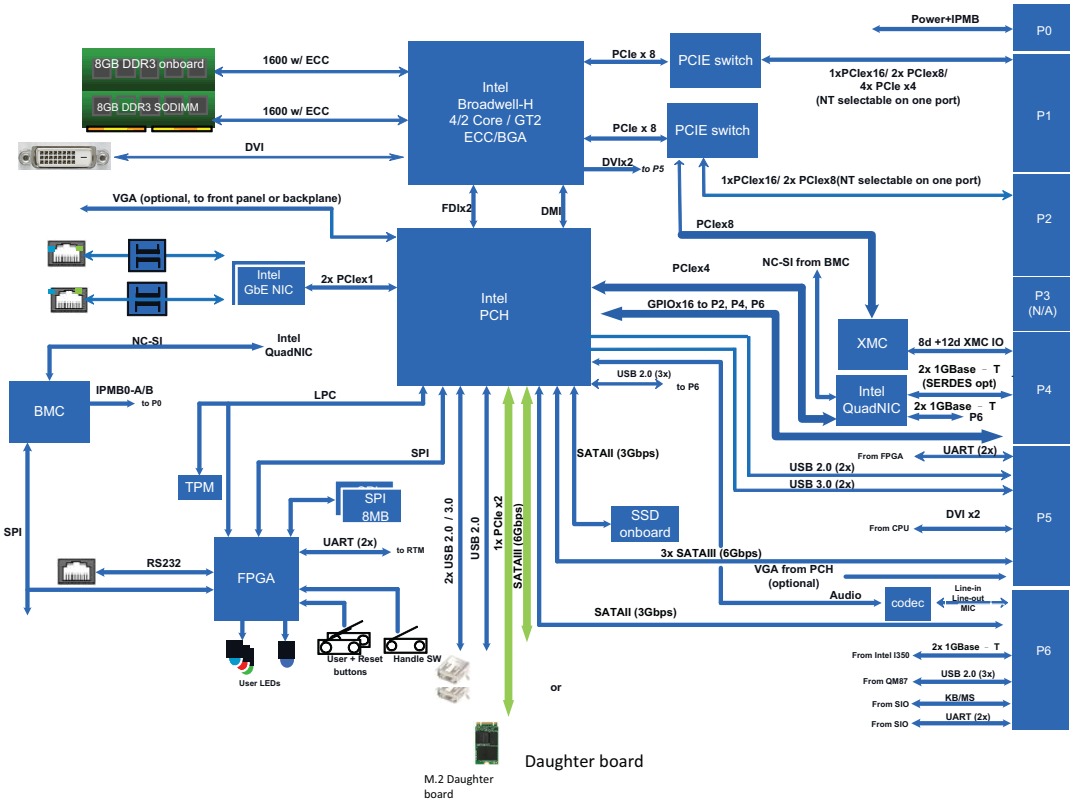


Figure 1.1 MIC-6314 functional block diagram

1.4 Board Map

The location of the main components, jumpers, switches, and thermal sensors is shown in the figure below.

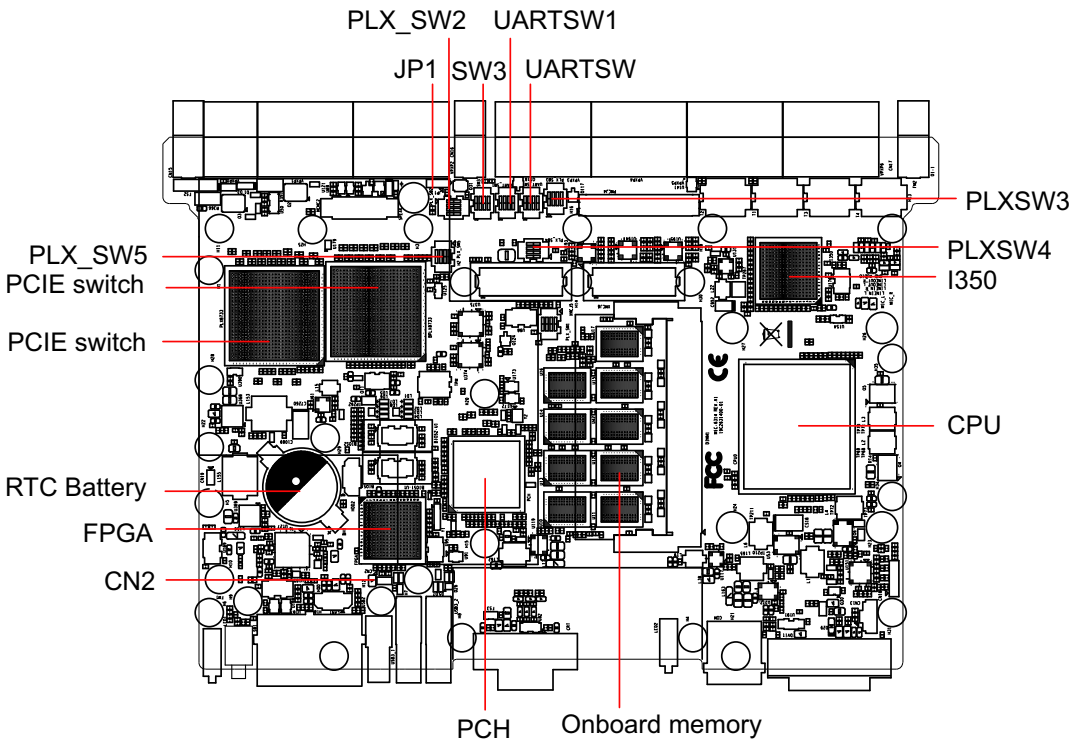


Figure 1.2 Board map

1.5 Jumpers and Switches

Table 1.4 and Table 1.5 list the jumper and switch functions. Read this section carefully before changing the jumper and switch settings on your MIC-6314 board.

Table 1.3: MIC-6314 Jumper Description

Number	Function
JP1	XMC VIO
CN2	Clear CMOS

Table 1.4: MIC-6314 Switch Description

Number	Function
FPGA_SW1	This switch is for the backplane LAN
PLX_SW2	This switch is for the PCIe configuration of the Expansion Plane (P2)
PLX_SW5	This switch is for the PCIe configuration of the Data Plane (P1)
UART_SW	RIO COM RS232/RS485/ RS422 mode selection
UART_SW1	
SW3	Front COM and RTM COM1/COM2 port selection for SIO UART

1.5.1 Clear CMOS (CN2)

This jumper is used to erase CMOS data. Follow the procedures below to clear the CMOS:

1. Turn off the system
2. Close jumper CN2 for approximately 3 seconds
3. Set jumper CN2 as Normal
4. Turn on the system. The BIOS is reset to its default settings

Table 1.5: CN2 Clear RTC		
	Closed	Clear RTC
Default	Open	Normal

1.5.2 XMC VIO Setting (JP1)

This jumper is used for setting the XMC IO voltage.

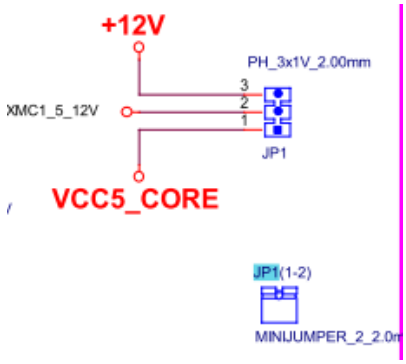


Figure 1.3 JP11 for XMC VIO (+5V or +12V)

Table 1.6: P11 for XMC VIO (+5V or +12V)		
JP1	Short 1,2 (default)	Short 2,3
XMC VPWR	5V	12V

1.5.3 Switch Settings

Note! ■ *Represents the key.*

Table 1.7: Backplane LAN Configuration	
LAN configure to copper	LAN configure to SerDes
FPGA_SW1 ON 4 (Default)	FPGA_SW1 ON 4

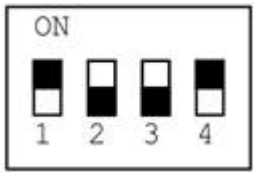
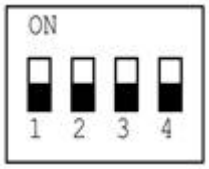
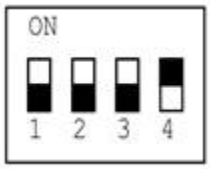
Table 1.8: PCIe configuration of the Expansion Plane (P2)		
X8 *2	X4 *4	X16 *1
PLX_SW2 (default)	PLX_SW2	PLX_SW2
		

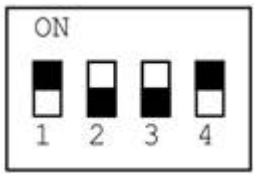
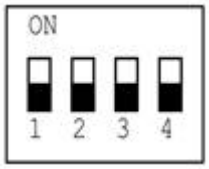
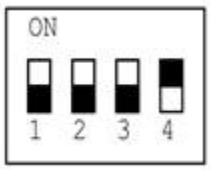
Table 1.9: PCIe configuration of the Data Plane (P1)		
X8 *2	X4 *4	X16 *1
PLX_SW5 (default)	PLX_SW5	PLX_SW5
		

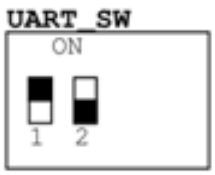
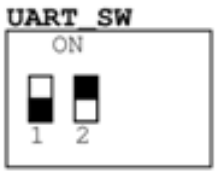
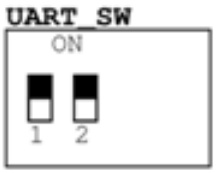
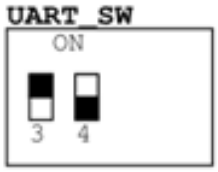
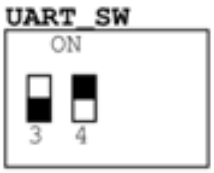
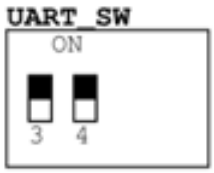
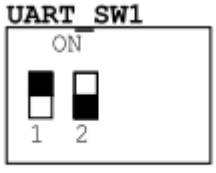
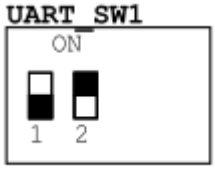
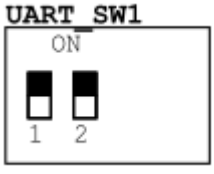
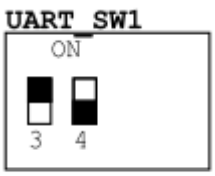
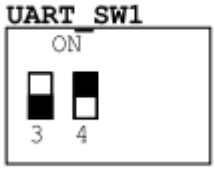
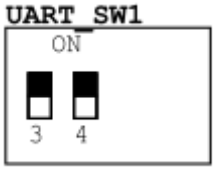
Table 1.10: RIO COM RS232/RS485/RS422 Mode Selection		
COM1 to backplane is set to RS232	COM1 to backplane is set to RS485	COM1 to backplane is set to RS422
		
COM2 to backplane is set to RS232	COM2 to backplane is set to RS485	COM2 to backplane is set to RS422
		
COM3 to backplane is set to RS232	COM3 to Backplane is set to RS485	COM3 to backplane is set to RS422
 (Default)		
COM4 to backplane is set to RS232	COM4 to backplane is set to RS485	COM4 to backplane is set to RS422

Table 1.10: RIO COM RS232/RS485/RS422 Mode Selection



(Default)





The COM ports that are routed to the backplane can be configured to three different console modes. The position of the keys must be selected at the correct “ON” orientation. BMC can use an OEM command to set the COM port configuration, but the setting will roll back to the FPGA default configuration at every boot up.

Table 1.11: SW3 Front COM and RTM COM1/COM2 Port Selection for BMC/SIO UART

Default	Front COM for BMC RTM COM1 for SIO COM1 RTM COM2 for SIO COM2	 (Default)
	Front COM for SIO COM1 RTM COM1 for BMC RTM COM2 for SIO COM2	
	Front COM for SIO COM2 RTM COM1 for SIO COM1 RTM COM2 for BMC	

1.6 Connector Definitions

Table 1.13 lists the function of every connector. Figures 1.3 and 1.4 show the location of every connector.

Table 1.12: MIC-6314 Connector Description

Number	Function
CNSATA1	SATA HDD daughter board
J15	XMC
CNDIMM	SODIMM socket

Figure 1.4 MIC-6314 front panel ports, indicators, and buttons

MIC-6314 supports three BMC-controlled front panel LEDs.

Table 1.13: Front Panel LEDs

LED	Color	Description
1	Blue	Hot-swap capability indicator
2	Green	BMC indicator
3	Green	Flashing = FW application active, payload (x86) in sleep Solid = FW application active, payload (x86) active

The LED behaviors are explained below.

Item	Meaning	Color	Behavior
Power	Power on	Green	LED on
HDD	HDD active	Yellow	Blinking
Hot swap	Ready to perform hot swap	Blue	LED on
BMC act LED	BMC active	Green	LED on

1.6.1 USB Connectors

MIC-6314 provides both USB 3.0 and USB 2.0 channels. The front panel features two USB 3.0 ports (USB 1 and USB 2) and one USB 2.0 port. Two USB 2.0 and USB 3.0 channels are routed to the P5 connector, and five USB 2.0 channels to the P6 connector. The USB interface provides complete plug-and-play functionality, as well as hot attach/detach capability for up to 127 external devices. The MIC-6314 USB interface complies with USB specifications, R 3.0, and is fuse protected (5V @ 1.1A). The USB interface can be disabled in the system BIOS setup. The USB controller default is set to “Enabled”.

1.6.2 Serial Ports

MIC-6314 features one serial port and two serial ports routed to P5. These ports are available as RS232 interfaces via RJ45 connectors on the front panel. RJ424/485 mode can be selected using the UART_SW switch. An RJ45 to DB-9 adaptor cable is provided in the MIC-6314 accessories to facilitate connection to an external console or modem devices. The BIOS Advanced Setup program described in Chapter 2 provides a user interface for enabling or disabling the ports and setting the port address. Many serial devices implement the RS232 standard in different ways. If you have problems with a serial device, check the connector pin assignments shown in Table 1.11. The IRQ and address range for these ports are fixed. However, if you wish to disable the port or change these parameters later, you can do this in the system BIOS setup.

1.6.3 Ethernet Configuration

MIC-6314 is equipped with a high-performance, PCI-Express-based, network interface controller, the I350, which provides fully compliant IEEE802.3 10/100/1000Base-TX Ethernet interfaces. Two GbE interfaces are connected to the front panel, and another two GbE interfaces are routed to the backplane. The two GbE connected to the backplane can be configured to SerDes. Please contact your local Advantech representative to inquire about the availability of the SerDes SKU.

1.6.4 SATA Daughter Board Connector (HDD/Extension Module)

MIC-6314 provides one SATA interface via the HDD connector for a daughter card for a CFast card, or optional onboard HDD. Four SATA (3.0 x3; 2.0 x1) interfaces are connected to the RIO for additional SATA HDDs.

1.6.5 System Reset and BMC Reset Button

MIC-6314 features a system reset button located on the front panel. The system reset button resets all payload and application-related circuitry, but does not reset the system management (IPMI) related circuitry. A separate BMC reset button on the front panel is provided for the BMC and related hardware.

1.7 Safety Precautions

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electric shock, always disconnect the power from the VPX chassis before manual handling. Do not touch any components on the CPU board or other boards while the VPX chassis is powered on.
- Disconnect the power before making any configuration changes. The sudden rush of power as a jumper is connected or a board installed may damage sensitive electronic components.
- Always ground yourself to remove any static charge before touching the CPU board. Be particularly careful not to touch the chip connectors.
- Modern integrated electronic devices, especially CPUs and memory chips, are extremely sensitive to static electric discharges and fields. Keep the board in the anti-static packaging when not installed in the chassis. When working with the board, place it on a static dissipative mat. Wear a grounding wrist strap for continuous protection.

1.8 Installation Steps

The MIC-6314 contains electro-statically sensitive devices. Please discharge your clothing before touching the assembly. Do not touch components or connector pins Advantech recommends that you perform assembly at an anti-static workbench.

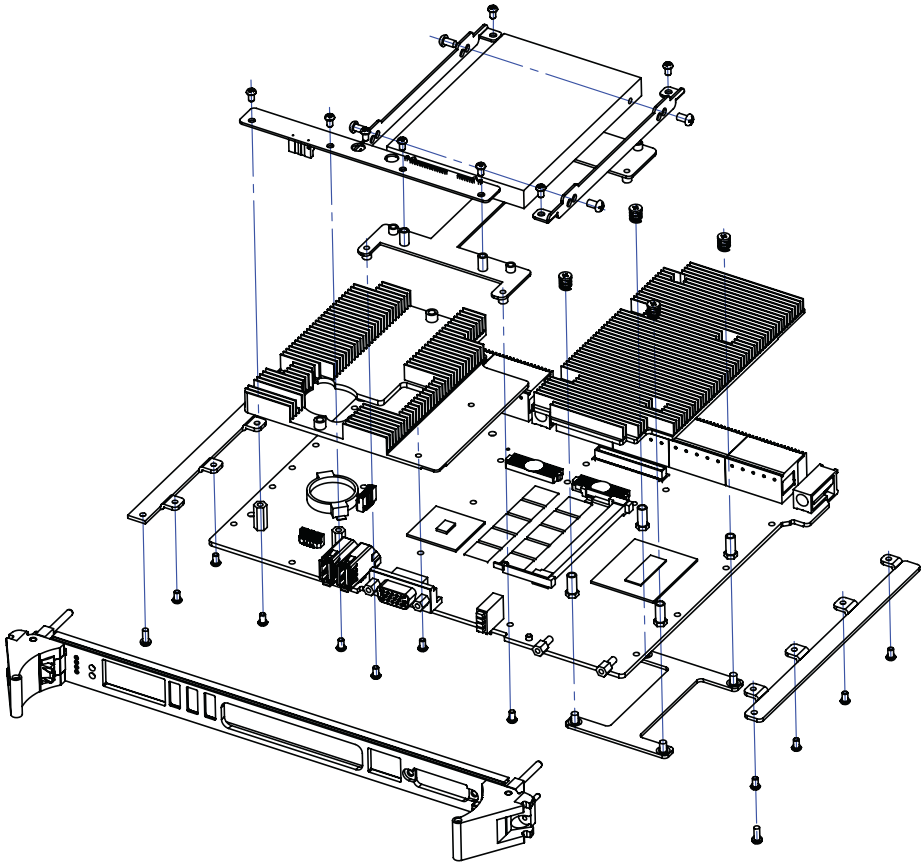


Figure 1.5 Complete assembly of MIC-6314 convection with the SATA daughter board

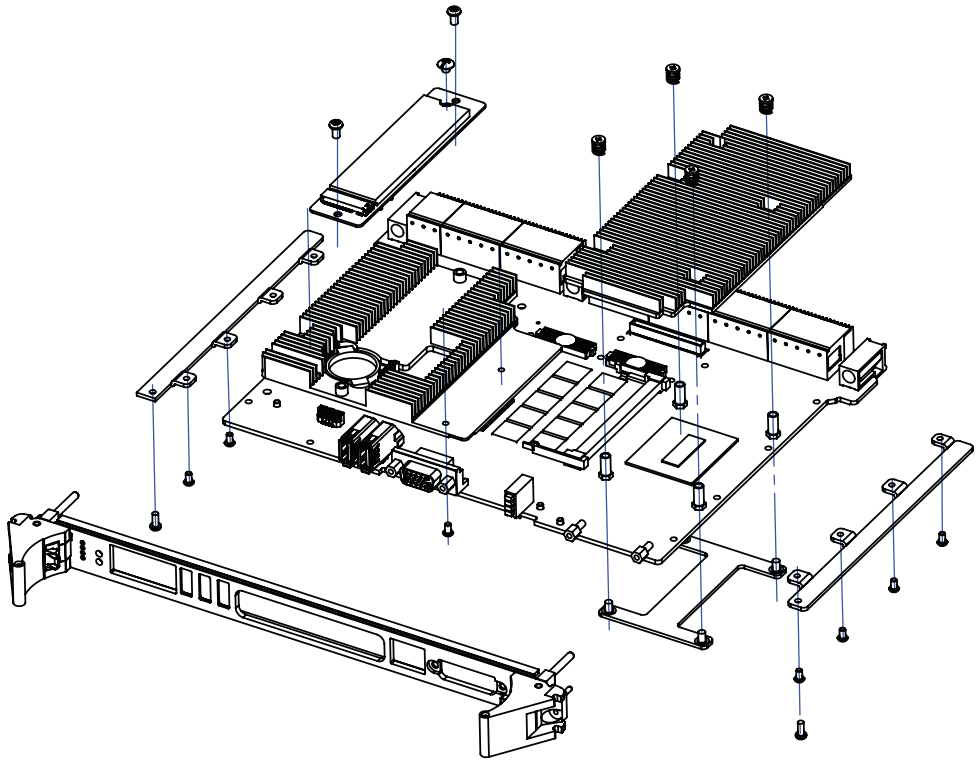


Figure 1.6 Complete assembly of MIC-6314 convection with the M.2 daughter board

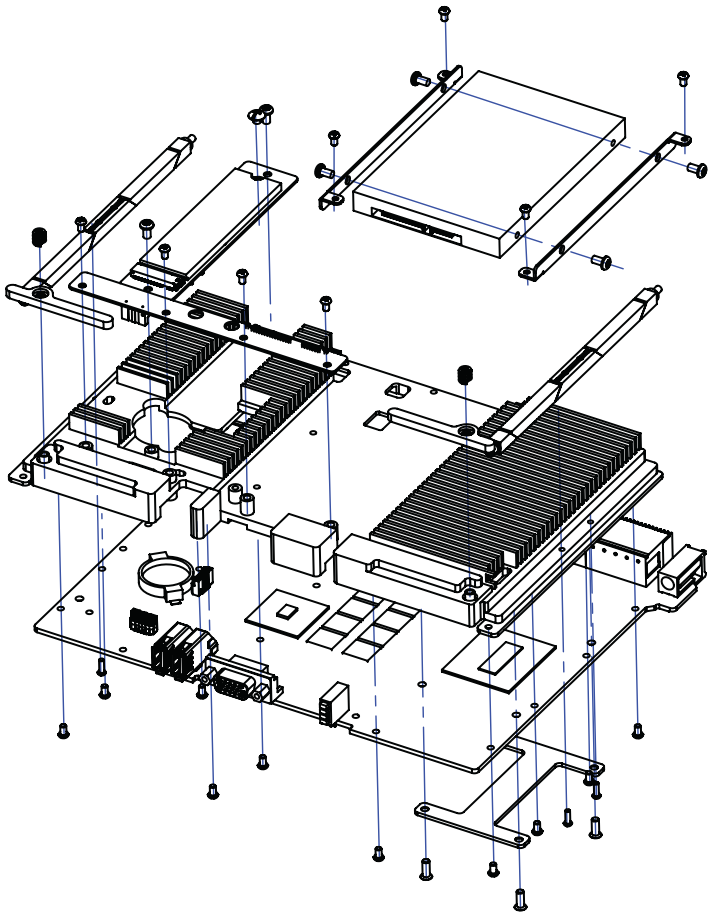


Figure 1.7 Complete assembly of MIC-6314 ruggedized convection with the M.2 daughter board

1.9 Battery Replacement

The battery type is a 3V, 210 mAh battery (model number CR2032M1S8-LF). Replacement batteries may be purchased from Advantech. Contact your local Advantech sales office to check the availability.

1750129010 – Battery 3V/210 mAh with wire assembly CR2032M1S8-LF

1.10 Software Support

Windows 7 and Red Hat Enterprise Linux have been fully tested on MIC-6314. Please contact your local Advantech sales representative to inquire about support for other operating systems.

1.11 Power consumption

The following data provide the maximum continuous current based on Advantech's verification result. These values include the margins to guarantee the behavior in the worst case.

Table 1.14: MIC-6314 power consumption

Power input	Max. load (A)	Note
12V	5.5	No load on the XMC site, the user should take into account the XMC's power consumption.
5V	1.35	

Table 1.15: MIC-6314 XMC site power budget

Power input	Max. load (A)	Note
12V	3	These values are based on the result of the power verification only. The user may need some specific heat dissipation solution to dissipate the heat according to the applied XMC.
5V	3	

Chapter 2

AMI APTIO BIOS Setup

This chapter describes how to configure the AMI APTIO BIOS (UEFI BIOS).

2.1 Introduction

To extend the features of the Intel® Grantley Platform, Advantech has equipped MIC-6314 with the latest AMI APTIO BIOS for enhanced performance.

The UEFI-compliant AMI APTIO BIOS is specifically adapted to MIC-6314 is described in this chapter. With the AMI APTIO BIOS Setup program, users can modify the BIOS settings and control the system's unique features. The setup program comprises a number of menus for implementing changes and enabling or disabling features. This chapter explains the basic navigation of the MIC-6314 setup screens.

The BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. Full instructions are provided in the following sections.

2.2 Entering Setup

Upon turning on the computer, the system show display a "patch" code that shows the BIOS supporting the CPU. This ensures that the CPU system status is valid. After ensuring that a number is assigned to the patch code, press <DEL> or <ESC> to enter setup.

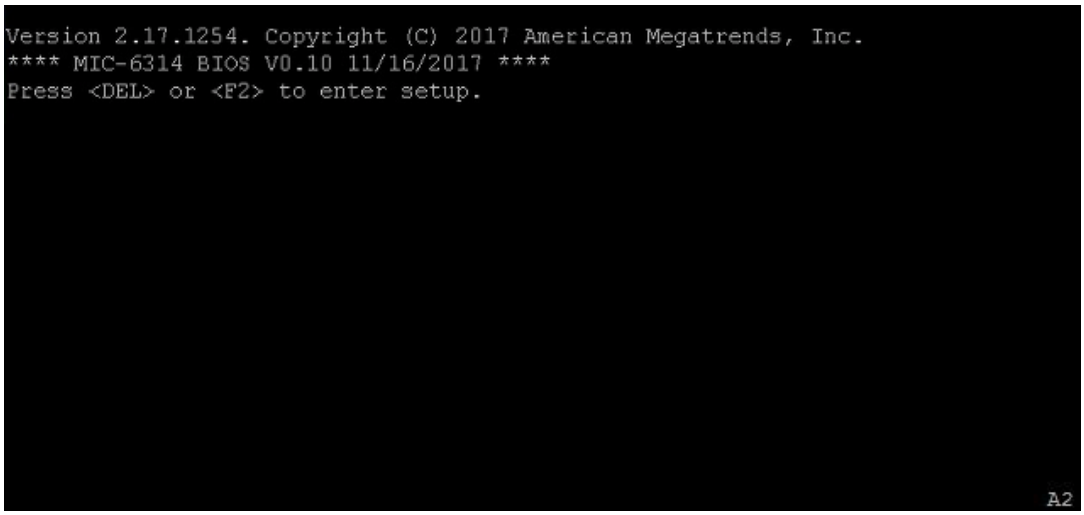


Figure 2.1 Press <DEL> or <ESC> to enter setup

2.2.1 Main Setup

Upon first accessing the BIOS Setup Utility, users will enter the Main setup screen. Users can always return to the Main setup screen by selecting the Main tab. Two main setup options are described in this section. The main BIOS setup screen is shown below.

The main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured (the default setting is shown in bold). The right frame displays the key legend. Above the key legend is an area reserved for a text message.

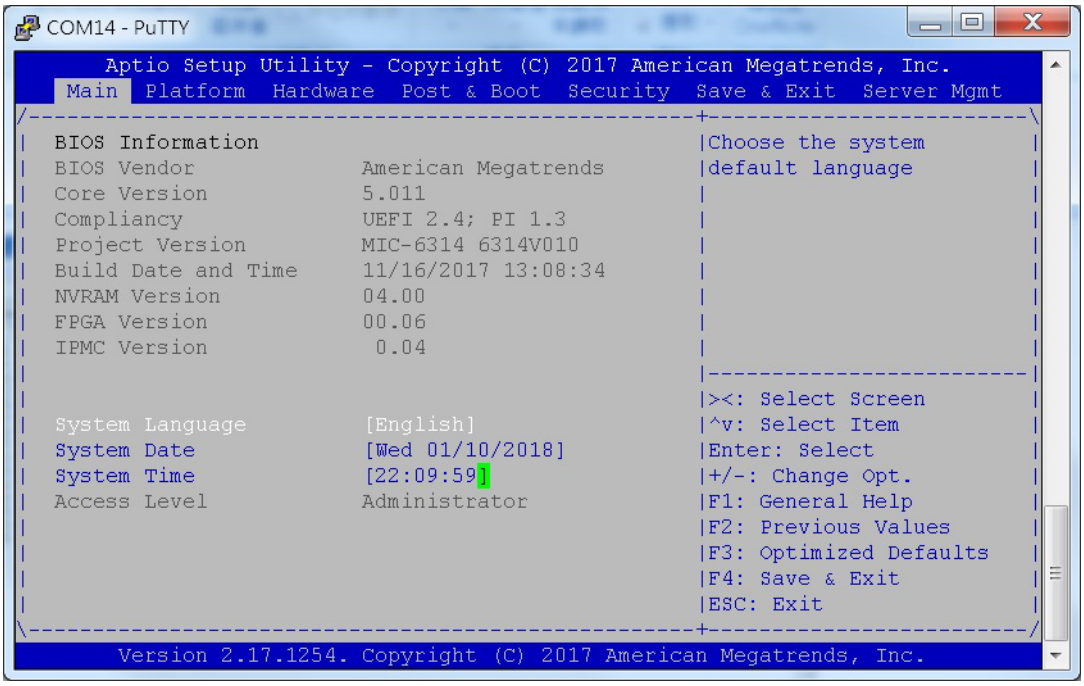


Figure 2.2 Main setup screen

Table 2.1: BIOS Menu: Main

Item	Options	Description	Help Text
BIOS Vendor	American Megatrends	BIOS vendor	N/A
Core Version	X.YYY	Show the BIOS core version	N/A
Compliance	UEFI X.Y; PI W.Z	Show the UEFI platform initialization version	N/A
Project Version	MIC-6314 6313XYYY	Show the BIOS version	N/A
Build Date/Time	mm/dd/yyyy hh:mm:ss	Show the BIOS build date and time	N/A
NVRAM Version	XX.YY	Show the NVRAM version	N/A
FPGA Version	XX.YY	Show the FPGA firmware version	N/A
IPMC Version	XX.YY	Show the IPMC firmware version	N/A
System Time	HH:MM:SS	Sets the system time	Use [+] or [-] for configuration
System Date	MM/DD/YYYY	Sets the system date	Use [+] or [-] for configuration
Access Level	Administrator/User	Display the current access level	

- **System Date/System Time**

  Use this option to change the system date or time. Highlight System Date or System Time by using the <Arrow> keys. Enter new values via the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

2.2.2 Platform Setup

Select the Platform tab from the MIC-6314 setup screen to enter the Platform setup screen. Users can select any of the items in the left frame of the screen, such as Serial Console, to access the submenu for that item. Users can display the Platform setup option by highlighting it using the <Arrow> keys. All Platform setup options are described in this section. The Platform setup screen is shown below. The submenus are described in the following pages.

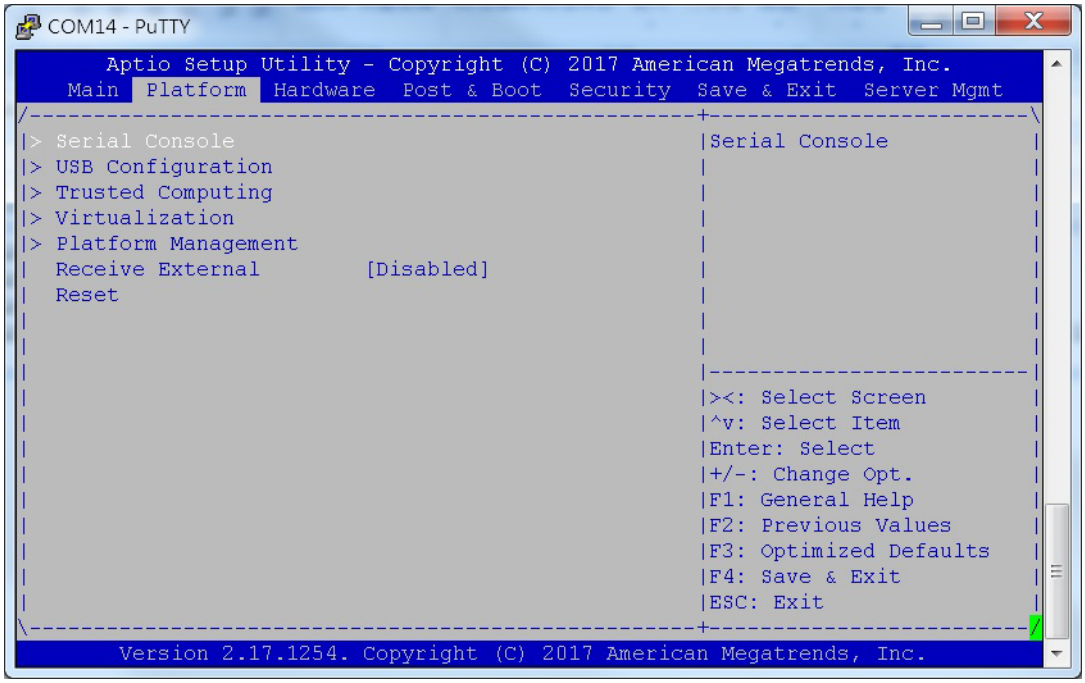


Figure 2.3 Platform setup screen

Table 2.2: Platform configuration

Item	Options	Description	Help Text
Serial Console		Enter “Serial Console” sub-menu	Serial Console
USB configuration		Enter “USB configuration” sub-menu	USB configuration
Trust Computing		Enter “Trust Computing” sub-menu	Trust Computing
Virtualization		Enter “Virtualization” sub-menu	Virtualization
Platform management		Enter “Platform management” sub-menu	Platform management
Received External Reset	Enable Disable	Receive the reset signal from the backplane, and perform reset behavior. This option is invalid when the module is in the system slot.	Receive External Reset

2.2.2.1 Serial Console

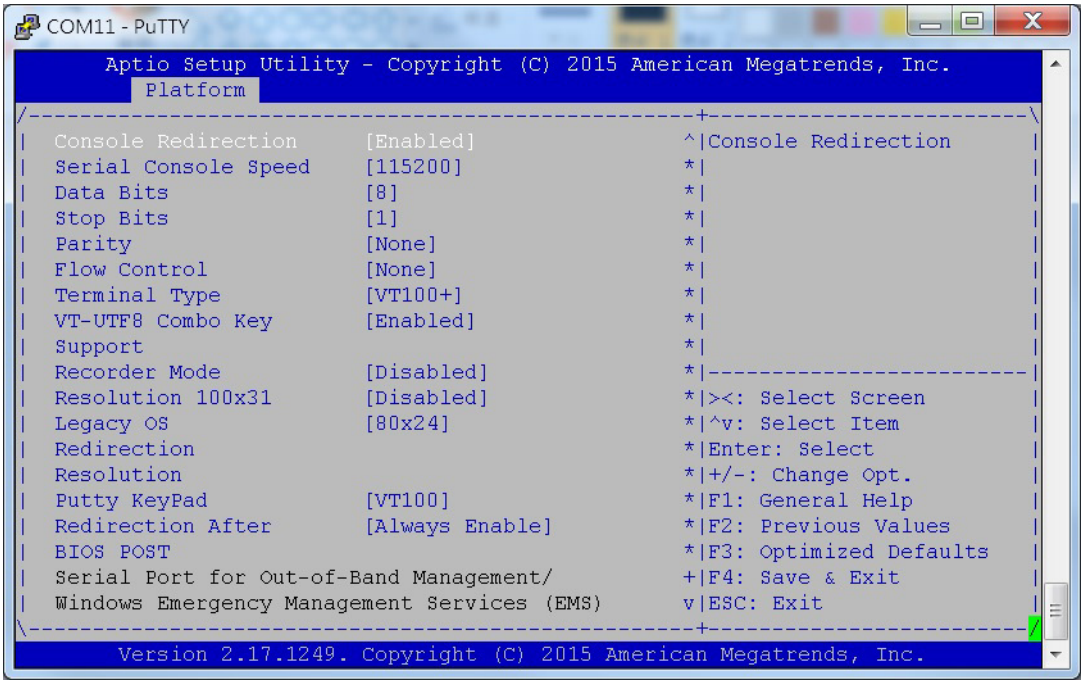


Figure 2.4 Serial console settings screen

Table 2.3: Serial Console Settings

Item	Options	Description	Help Text
Console Redirection	Enabled Disabled	Enable or disable console redirection.	Console redirection
Serial Console Speed	9600, 19200, 38400, 57600, 115200	Configure the serial port baud rate.	Select the serial port baud rate
Data Bits	7 8	Configure the number of data bits in each transmitted or received serial character for both serial ports.	Data bits
Stop Bits	1 2	Configure the number of stop bits transmitted and received in each serial character for both serial ports.	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

Table 2.3: Serial Console Settings			
Parity	None, Even, Odd, Mark, Space	Configure if parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data for both serial ports.	A parity bit can be sent with the data bits to detect transmission errors. Even: parity bit is 0 if the number of 1s in the data bits is even. Odd: parity bit is 0 if the number of 1s in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space parity do not allow for error detection. They can be used as an additional data bit.
Flow Control	None, Hardware RTS/CTS	Configure flow control for console redirection.	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a “stop” signal can be sent to stop the data flow. Once the buffers are empty, a “start” signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
Terminal Type	VT100, VT100+, VT-UTF8, ANSI	Configure the type of console emulation used.	Terminal Type for Redirection Via AMI Debugger. Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
VT-UTF8 Combo Key Support	Enabled, Disabled	Enable or disable the VT-UTF8 combo key.	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.
Recorder Mode	Enabled, Disabled	Configure the terminal display mode. If terminal function is used to capture text, the Recorder mode will not send ANSI codes (all data will be received like a video display).	With this mode is enabled, only text will be sent. This is to capture terminal data.

Table 2.3: Serial Console Settings			
Resolution 100 x 31	Enabled Disabled	Enable or disable extended terminal resolution.	Enable or disable extended terminal resolution.
Legacy OS Redirection Resolution	80x25, 80x24	Display the terminal size.	On legacy OS, the number of rows and columns support redirection.
Putty KeyPad	VT100 LINUX XTERMR6 SCO ESCN VT400	Select the FunctionKey and KeyPad on Putty.	Select the FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	Always Enable BootLoader	The settings specify that if BootLoader is selected, then legacy console redirection is disabled before booting to legacy OS. The default value is always Enabled which means legacy console redirection is enabled for legacy OS.	The settings specify that if BootLoader is selected, then legacy console redirection is disabled before booting to legacy OS. The default value is always Enabled which means Legacy Console Redirection is enabled for legacy OS.

2.2.2.2 USB Configuration

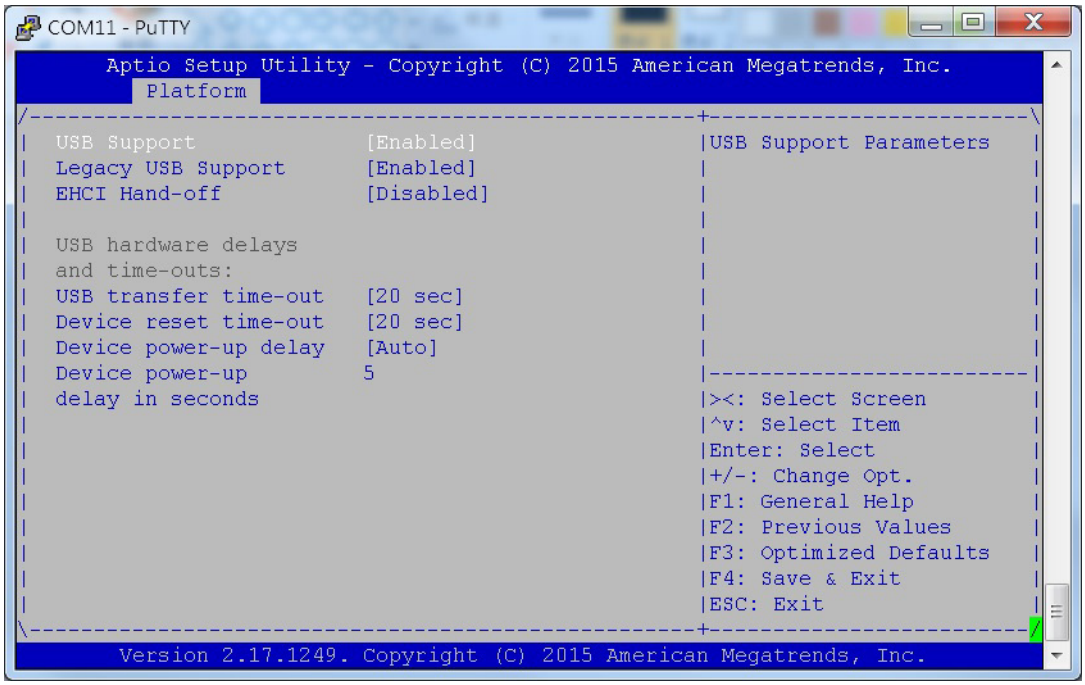


Figure 2.5 USB configuration screen

Table 2.4: USB Configuration

Item	Options	Description	Help Text
USB Support	Disabled Enabled	Enable or disable USB function support	USB support parameters
Legacy USB Support	Enabled Disabled Auto	Enable or disable legacy USB support. The Auto option disables legacy support if no USB devices are connected. The Disable option keeps USB devices available only for EFI applications.	The Auto option disables legacy support if no USB devices are connected. The Disable option keeps USB devices available only for EFI applications.
EHCI Hand-Off	Enabled Disabled	Enable or disable EHCI hand-offs for operating systems without ECHI hand-off support.	This is a workaround for operating systems without XHCI hand-off support. The XHCI ownership change should be claimed by the XHCI driver.
USB Transfer Timeout	1 sec 5 sec 10 sec 20 sec	Timeout value for Control, Bulk, and Interrupt transfers.	The timeout value for Control, Bulk, and Interrupt transfers.
Device Reset Timeout	1 sec 5 sec 10 sec 20 sec	USB mass storage device start unit command timeout.	USB mass storage device start unit command timeout.
Device Power-Up Delay		Maximum time the device will take before reporting itself to the host controller.	Maximum time the device will take before reporting itself to the host controller.

2.2.2.3 Trusted Computing

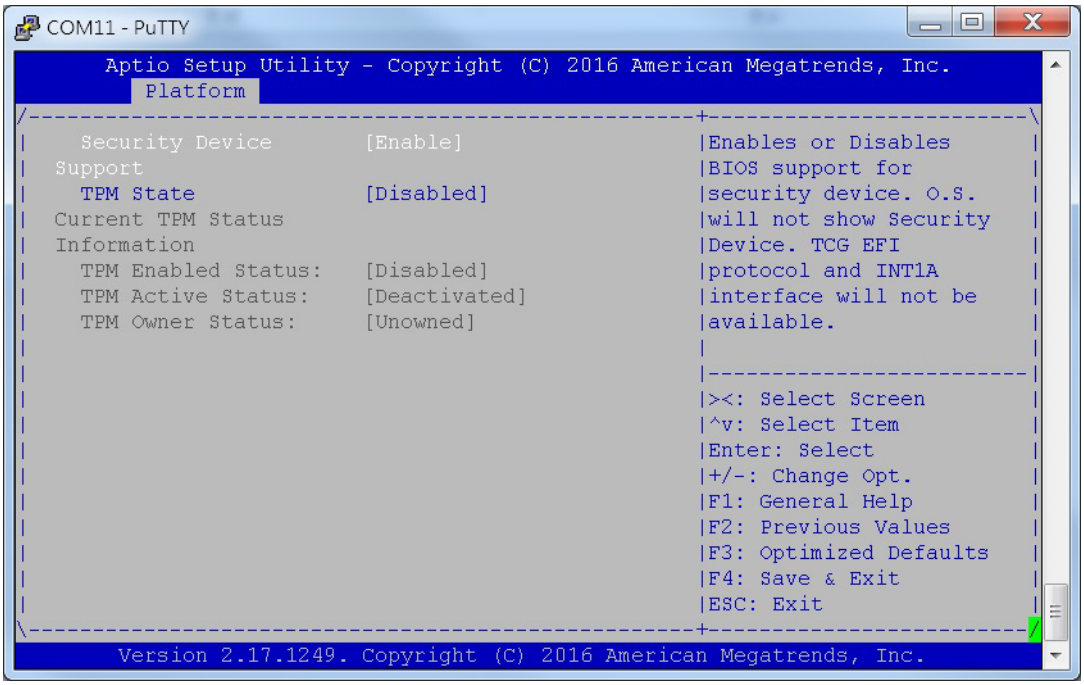


Figure 2.6 Trusted computing screen

Table 2.5: Trusted Computing

Item	Options	Description	Help Text
Security Device Support	Disabled Enabled	Enable or disable BIOS support for security devices. The OS will not show security devices. The TCG EFI protocol and INT1A interface will not be available.	Enable or disable BIOS support for security devices. The OS will not show security devices. The TCG EFI protocol and INT1A interface will not be available.
TPM State	Enabled Disabled	Enable or disable security devices.	The computer will reboot during restart to change the device state.

2.2.2.4 Virtualization

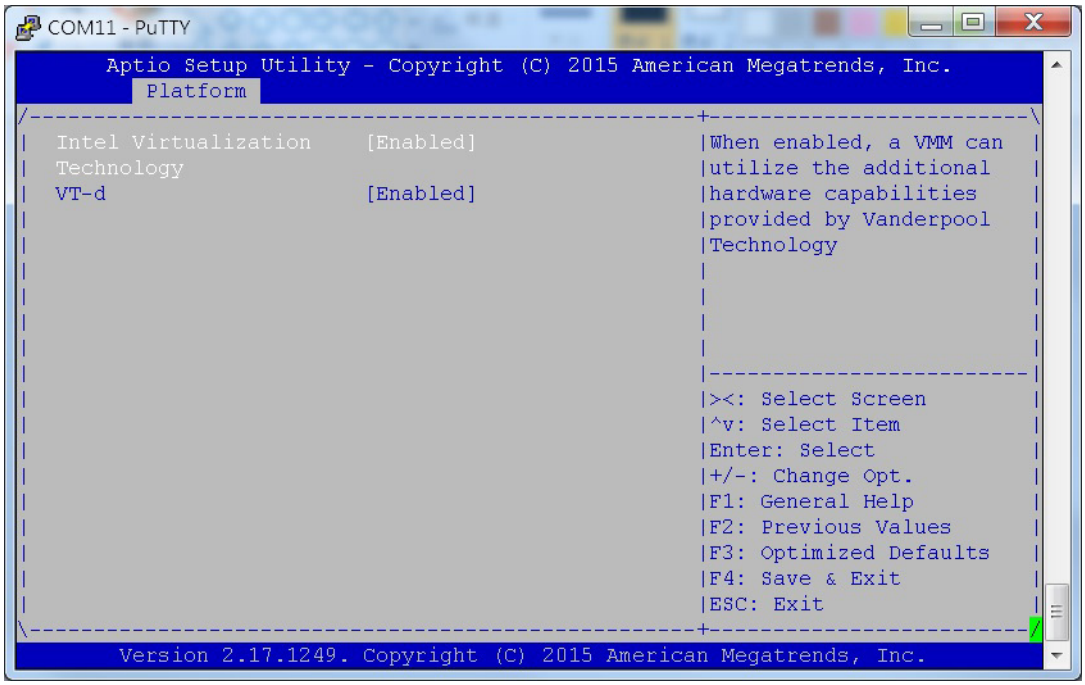


Figure 2.7 Virtualization settings screen

Table 2.6: Virtualization

Item	Options	Description	Help Text
Intel® Virtualization Technology	Disabled Enabled	Enable or disable BIOS support for Vanderpool Technology.	Enabling Vanderpool Technology will take effect after reboot.
Intel® VT-d	Enabled Disabled	Enable or disable Intel® Virtualization Technology for directed I/O (VT-d) by reporting the I/O device assignment to VMM through DMAR ACPI tables.	Enable or disable Intel® Virtualization Technology for directed I/O (VT-d) by reporting the I/O device assignment to VMM through DMAR ACPI tables.

2.2.2.5 Platform Management

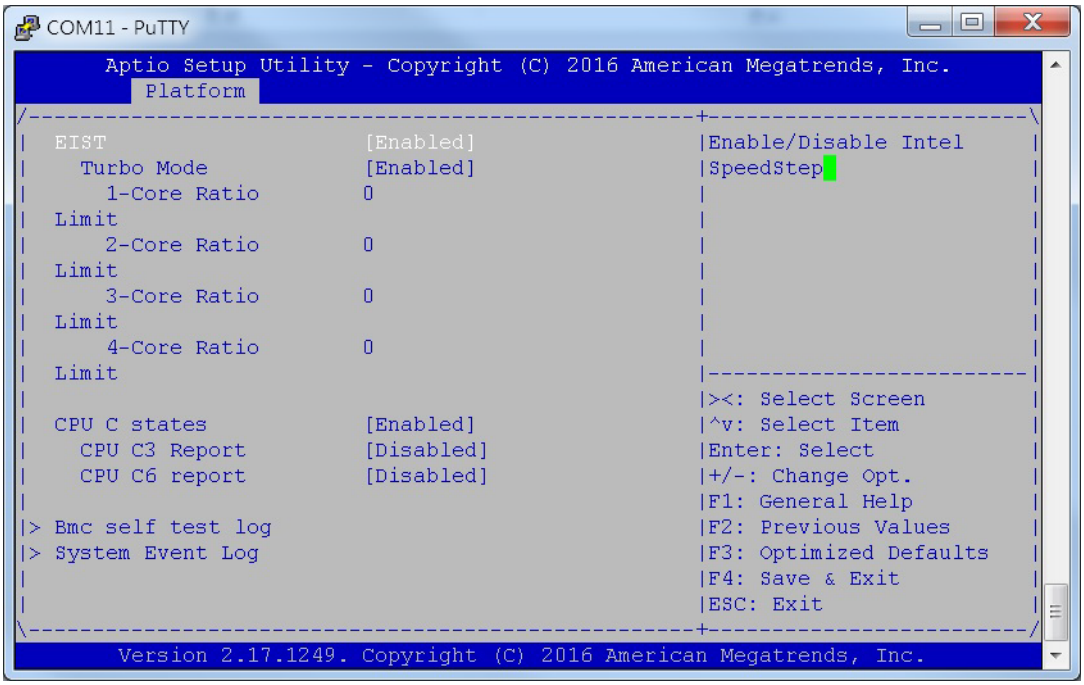


Figure 2.8 Platform management screen

Table 2.7: Platform Management

Item	Options	Description	Help Text
EIST	Disabled Enabled	Enable or disable BIOS support for Enhanced Intel® SpeedStep® Technology	When enabled, OS sets CPU frequency according load. When disabled, CPU frequency is set at max non-turbo.
Turbo Mode	Enabled Disabled	Enable or disable processor Turbo mode. Turbo mode allows a CPU logical processor to execute a higher frequency when enough power is available, without exceeding CPU defined limits.	Turbo mode allows a CPU logical processor to execute a higher frequency when enough power is available not exceed CPU defined limits.
CPU C States	Enabled Disabled	This option allows users to turn off unused components to save power.	Enable or disable CPU states.
CPU C3 Report	Enabled Disabled	Enable or disable CPU C3 report to OS.	Enable or disable CPU C3(ACPI C2) report to OS. The recommended setting is Disabled.
CPU C6 Report	Enabled Disabled	Enable or disable CPU C6 report to OS.	Enable or disable CPU C6(ACPI C2) report to OS. The recommended setting is Enabled.

BMC Self-Test Log

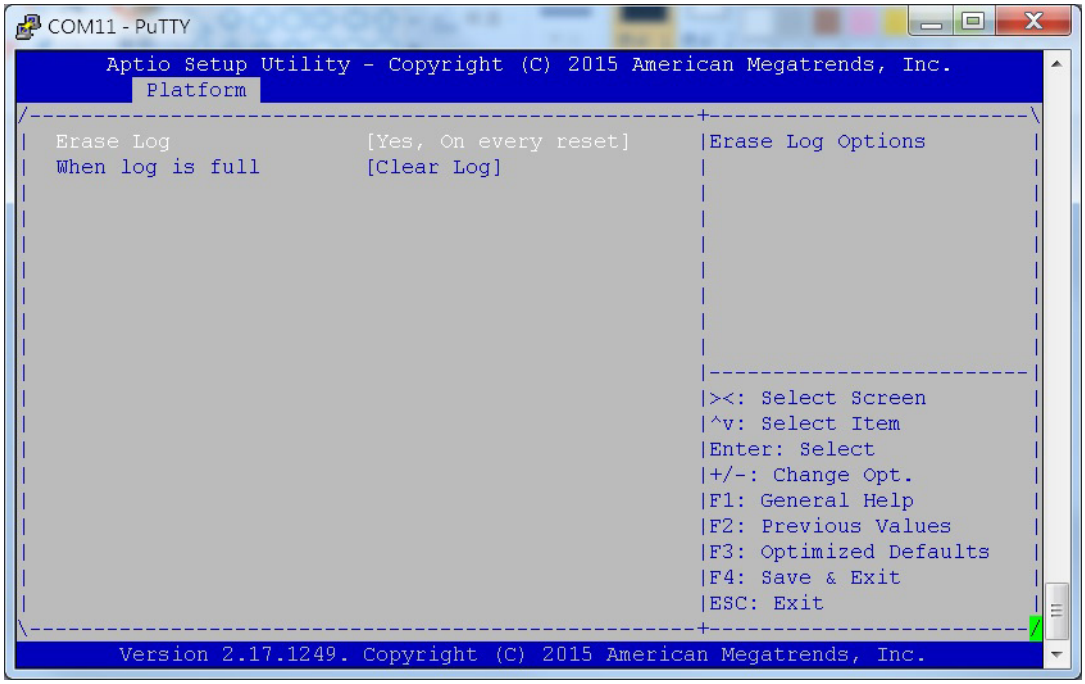


Figure 2.9 BMC self-test log screen

Table 2.8: BMC Self-Test Log

Item	Options	Description	Help Text
Erase Log	Yes, on every reset No	Decide if the log should be erased every time the blade reset.	Erase log options.
When Log is Full	Clear Log Do not log anymore	Select the behavior when the log is full.	Select the action to be taken when the log is full.

System Event log

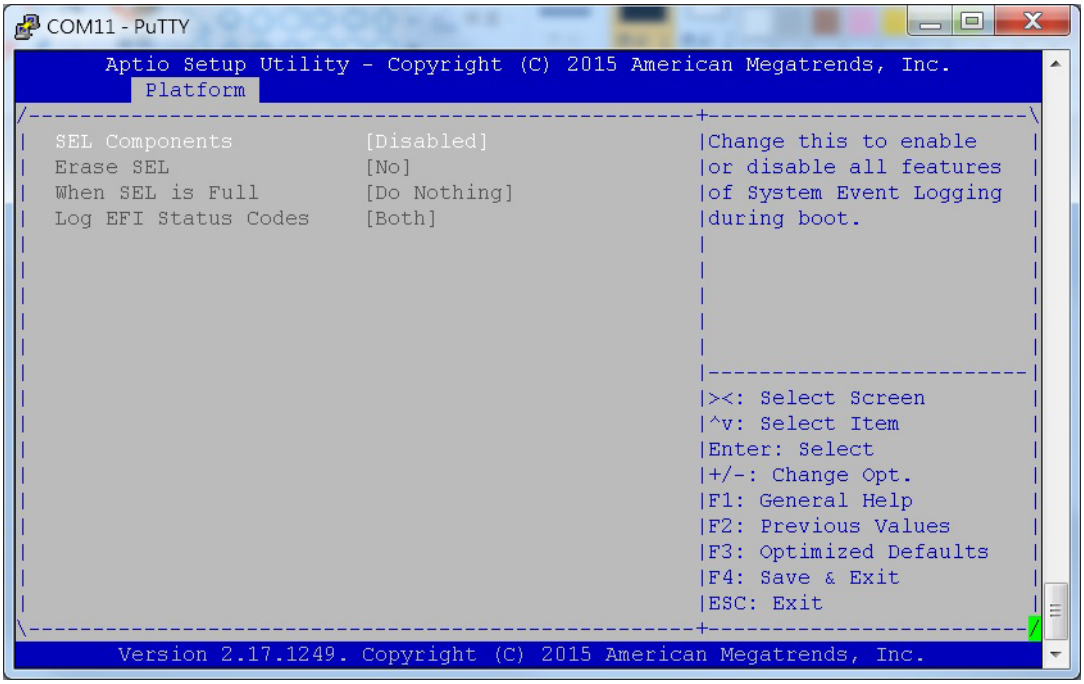


Figure 2.10 System event log screen

Table 2.9: System Event Log

Item	Options	Description	Help Text
SEL Components	Enabled Disabled	Enable or disable all the features of system event logging during boot.	Change this to enable or disable all the features of system event logging during boot.

2.2.3 Hardware Setup

Select the chipset tab from the MIC-6314 setup screen to enter the Hardware setup screen. Users can configure the CPU, northbridge, southbridge, Super IO, and HW monitor parameters.

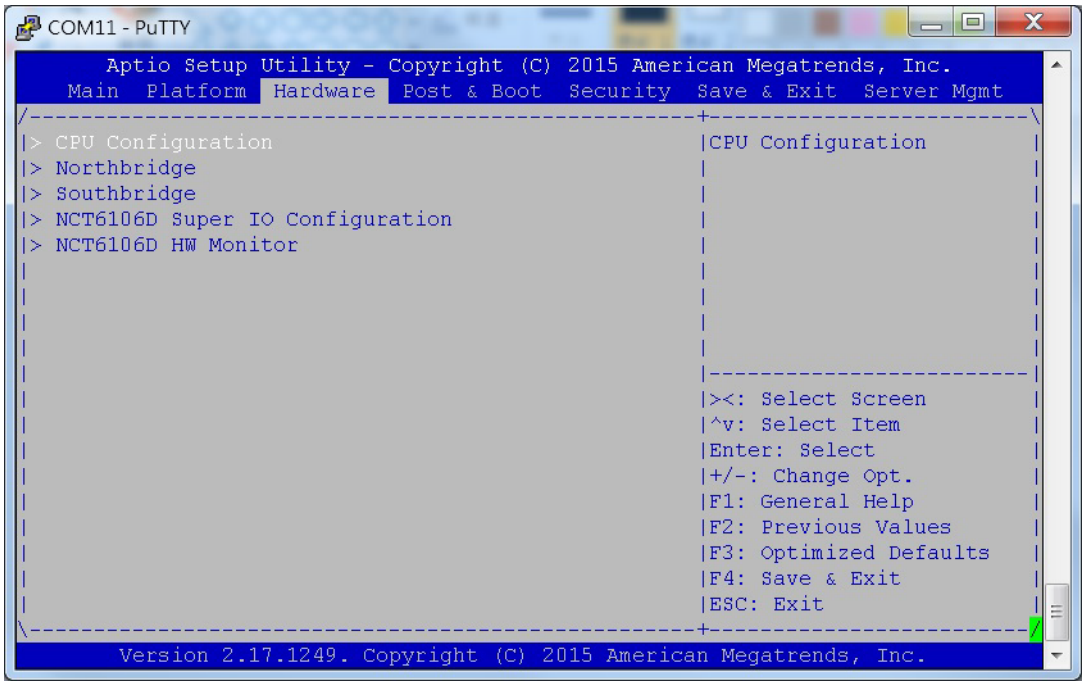


Figure 2.11 Hardware settings screen

2.2.3.1 CPU Configuration

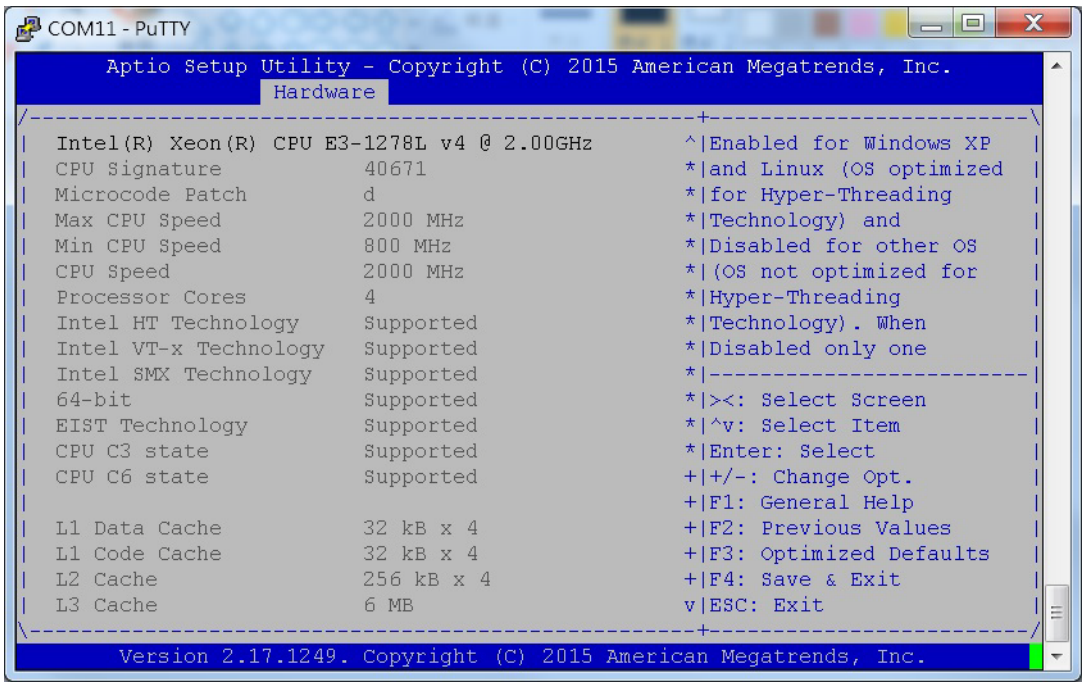


Figure 2.12 CPU configuration screen

2.2.3.2 Northbridge

Users can configure all the parameters related to the IOH function on the Northbridge setup page. The MIC-6314 BIOS also allows users to configure the PCIe link speed (Gen 1, 2, or 3) and its functions (x16, x8x8, x8x4x4, x4x4x8 or x4x4x4x4) on the IOH configuration submenu.

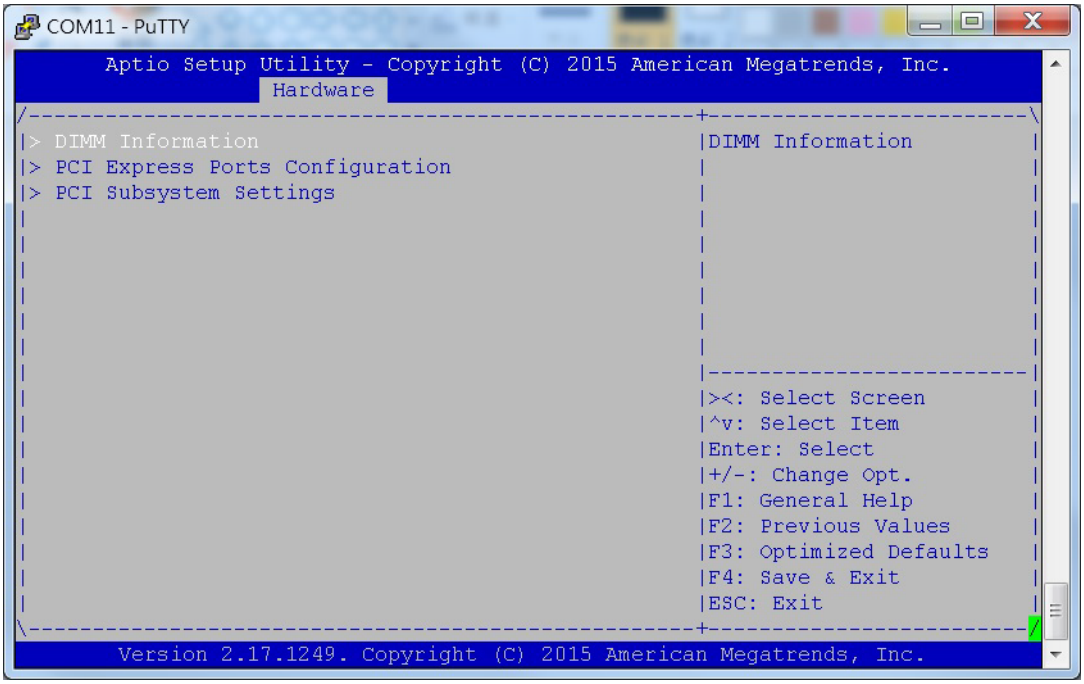


Figure 2.13 Northbridge configuration screen

- **DIMM Information**

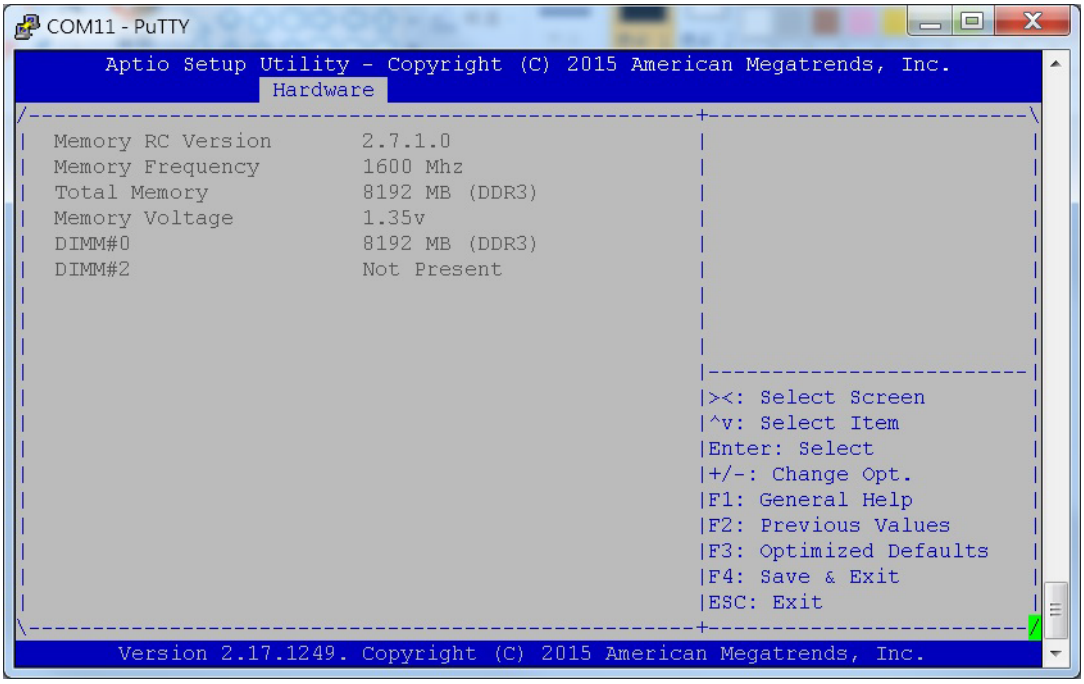


Figure 2.14 Memory configuration screen

PCI Express Port Configuration

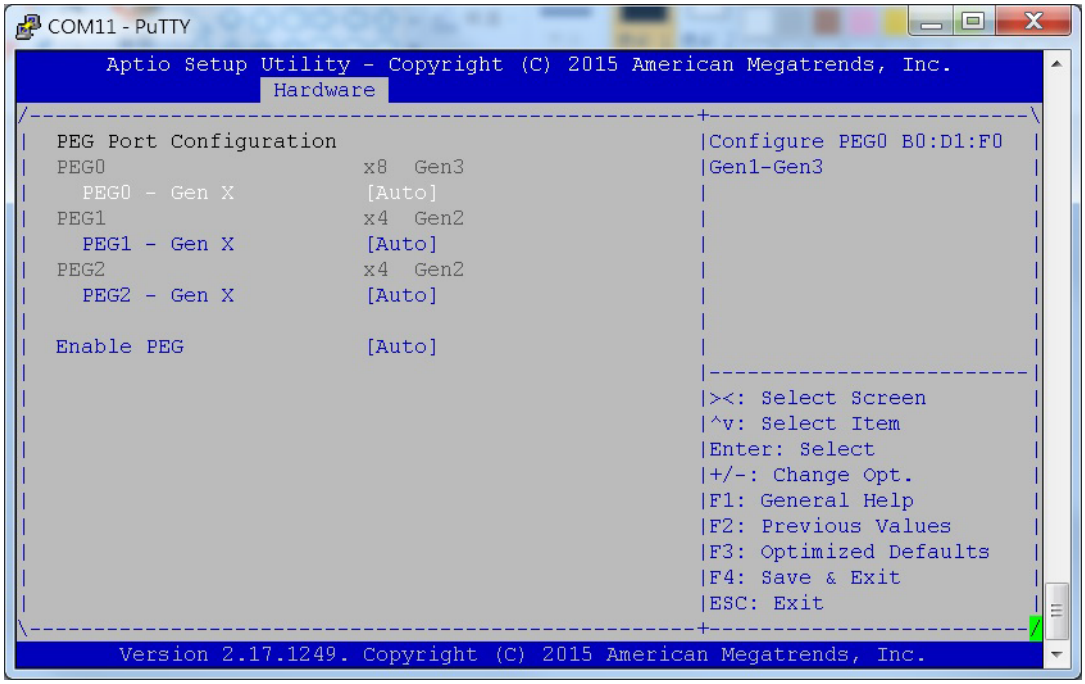


Figure 2.15 PCI Express port configuration screen

Table 2.10: PCI Express Port Configuration

Item	Options	Description	Help Text
PEG0/PEG1/ PEG2	Auto Gen1 Gen2 Gen3	Access PEG0/1/2 link and speed information.	Configure PEG0/1/2 B0:D1:F0 Gen1-Gen3.
Enable PEG	Auto Enable Disable	Enable or disable PEG.	Enable or disable PEG.

PCI Subsystem Settings

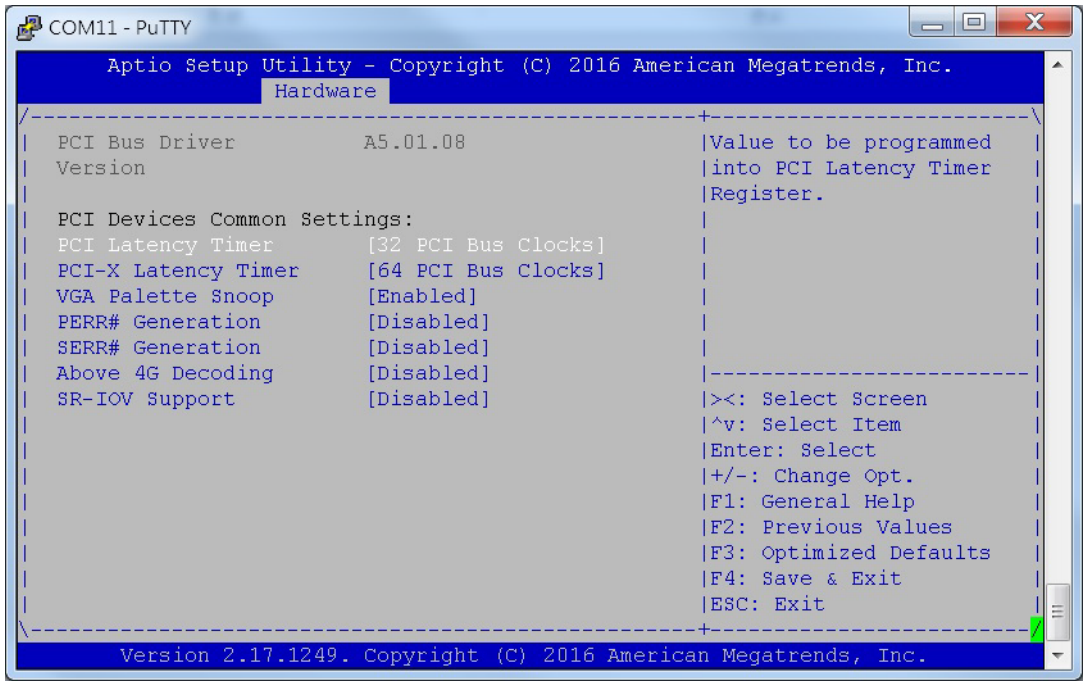


Figure 2.16 PCI subsystem setting screen

Table 2.11: PCI Subsystem Settings

Item	Options	Description	Help Text
PCI Latency Timer	32 PCI Bus Clocks 64 PCI Bus Clocks 96 PCI Bus Clocks 128 PCI Bus Clocks 160 PCI Bus Clocks 192 PCI Bus Clocks 224 PCI Bus Clocks 248 PCI Bus Clocks	Sets the value to be programmed into the PCI latency timer register.	Sets the value to be programmed into the PCI latency timer register.

Table 2.11: PCI Subsystem Settings			
PCI-X Latency Timer	32 PCI Bus Clocks 64 PCI Bus Clocks 96 PCI Bus Clocks 128 PCI Bus Clocks 160 PCI Bus Clocks 192 PCI Bus Clocks 224 PCI Bus Clocks 248 PCI Bus Clocks	Sets the value to be programmed into the PCI latency timer register.	Sets the value to be programmed into the PCI latency timer register.
VGA Palette Snoop	Disabled Enabled	Enable or disable VGA palette register snooping.	Enable or disable VGA palette register snooping.
PERR# Generation	Disabled Enabled	Enable or disable the PCI device from generating PERR#.	Enable or disable the PCI device from generating PERR#.,
SERR# Generation	Disabled Enabled	Enable or disable the PCI device from generating SERR#.	Enable or disable the PCI device from generating SERR#.
Above 4G Decoding	Disabled Enabled	Enable or disable 64-bit-capable devices from decoding in an above 4G address space (only if the system supports 64-bit PCI decoding).	Enable or disable 64-bit-capable devices from decoding in an above 4G address space (only if the system supports 64-bit PCI decoding).
SRIOV Support	Disabled Enabled	If the system has SR-IOV-capable PCIe devices, enable or disable single root IO virtualization support.	If the system has SR-IOV-capable PCIe devices, enable or disable single root IO virtualization support.

2.2.3.3 Southbridge

Users can configure all the parameters related to PCH function on the Southbridge setup page.

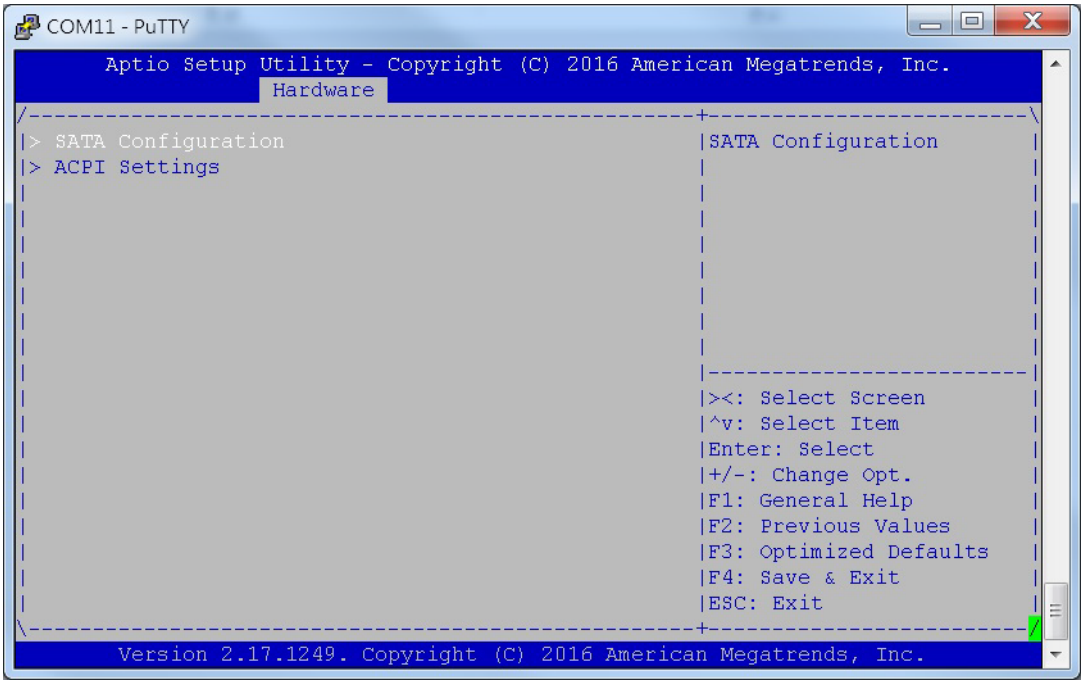


Figure 2.17 Southbridge configuration screen

- **SATA Configuration**

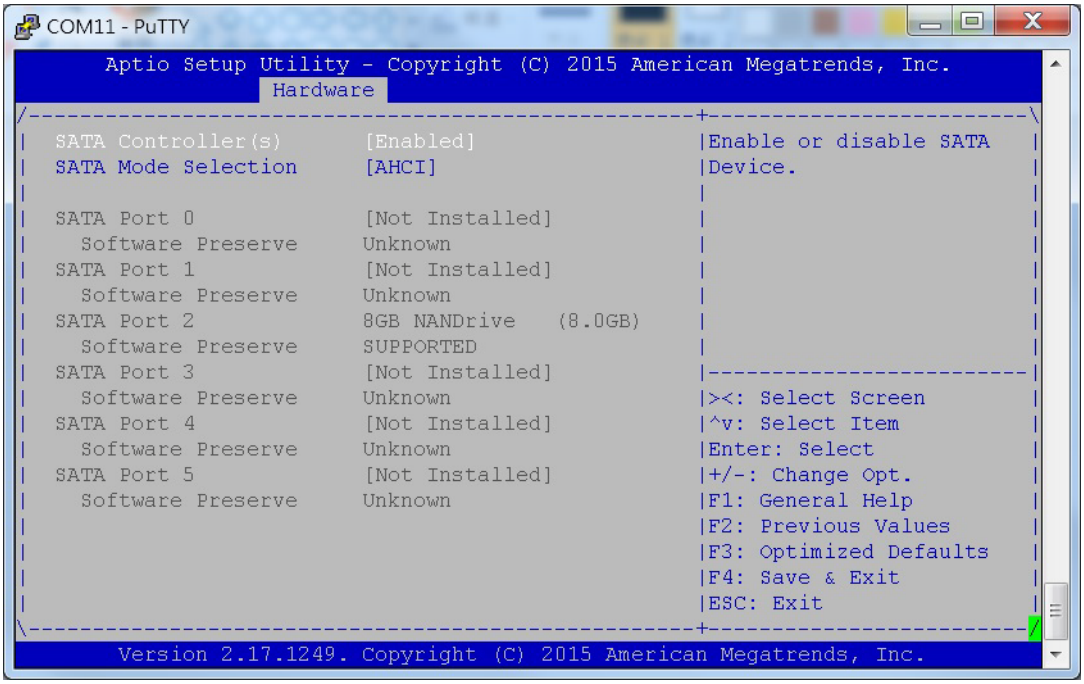


Figure 2.18 SATA configuration screen

Table 2.12: SATA Configuration			
Item	**Options**	**Description**	**Help Text**
SATA Controller	Disabled Enabled	Enable or disable the SATA controller.	Enable or disable the SATA controller.
SATA Mode	AHCI IDE	Configure SATA as IDE or AHCI.	Configure SATA as IDE or AHCI.

ACPI Settings

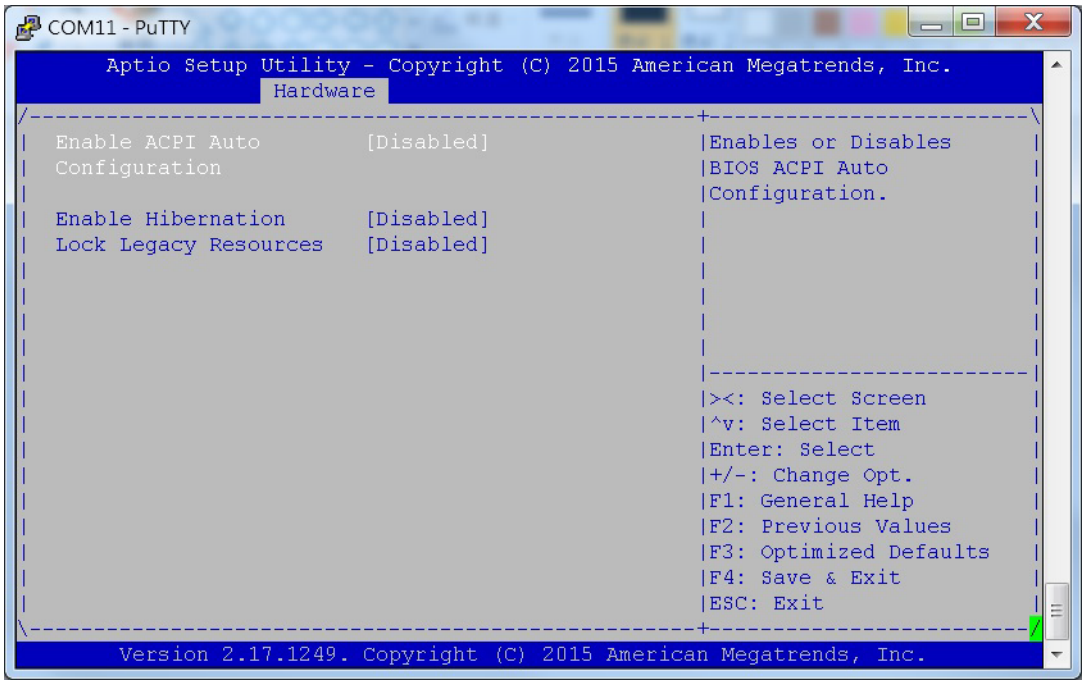


Figure 2.19 ACPI settings screen

Table 2.13: ACPI Settings			
Item	**Options**	**Description**	**Help Text**
Enable ACPI Auto Configuration	Disabled Enabled	Enable or disable BIOS ACPI auto configuration.	Enable or disable BIOS ACPI auto configuration.
Enable Hibernation	Disabled Enabled	Enable or disable system hibernation (OS/S4 Sleep State). This option may not be available with certain operating systems.	Enable or disable system hibernation (OS/S4 Sleep State).
Lock Legacy Resources	Disabled Enabled	Enable or disable legacy resource locking.	Enable or disable legacy resource locking.

2.2.3.4 NCT6106D Super IO Configuration

Users can configure the serial port parameters related to the NCT6104D Super IO.

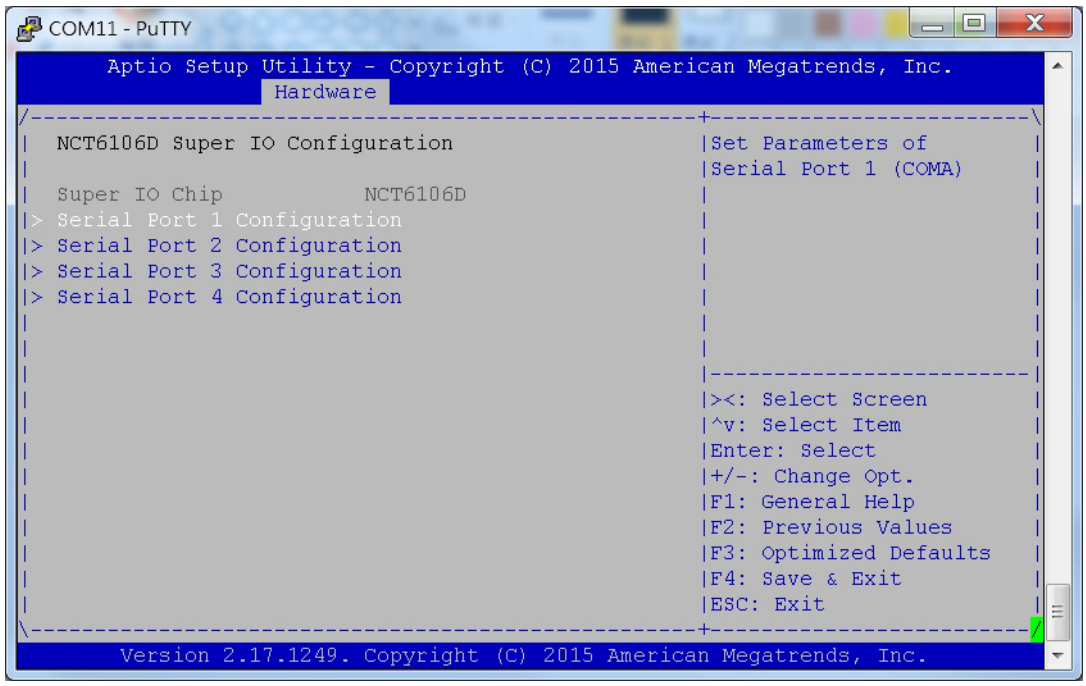


Figure 2.20 NCT6106D Super IO configuration screen

- **Serial Port 1/2/3/4 Configuration**

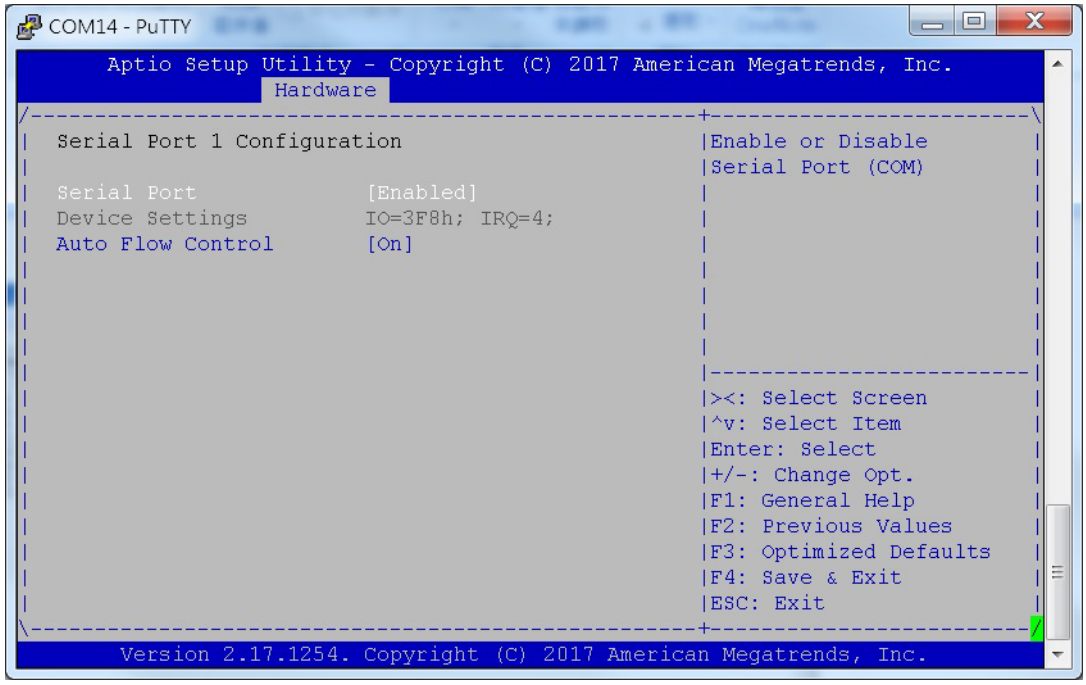


Figure 2.21 Serial port 1/2/3/4 configuration screen

Table 2.14: Serial Port 1/2/3/4 Configuration			
Item	**Options**	**Description**	**Help Text**
Serial Port	Disabled Enabled	Enable or disable serial ports (COM).	Enable or disable serial ports (COM).
Auto Flow Control	On Off	Enable or disable the Auto Flow Control of RS485 mode	Auto Flow Control

Table 2.15: SATA Configuration			
Item	**Options**	**Description**	**Help Text**
Serial Port	Disabled Enabled	Enable or disable serial ports (COM).	Enable or disable serial ports (COM).
Change Settings	Auto IO=3F8h; IRQ=4 IO=3F8h; IRQ=3,4,5,6 IO=2F8h; IRQ=3,4,5,6 IO=3E8h; IRQ=3,4,5,6 IO=2E8h; IRQ=3,4,5,6	Select the optimal setting for Super IO devices.	Select the optimal setting for Super IO devices.

2.2.3.5 NCT6106D HW Monitor

Users can access the data collected by the NCT6104D monitor sensors to monitor the blade system heath status.

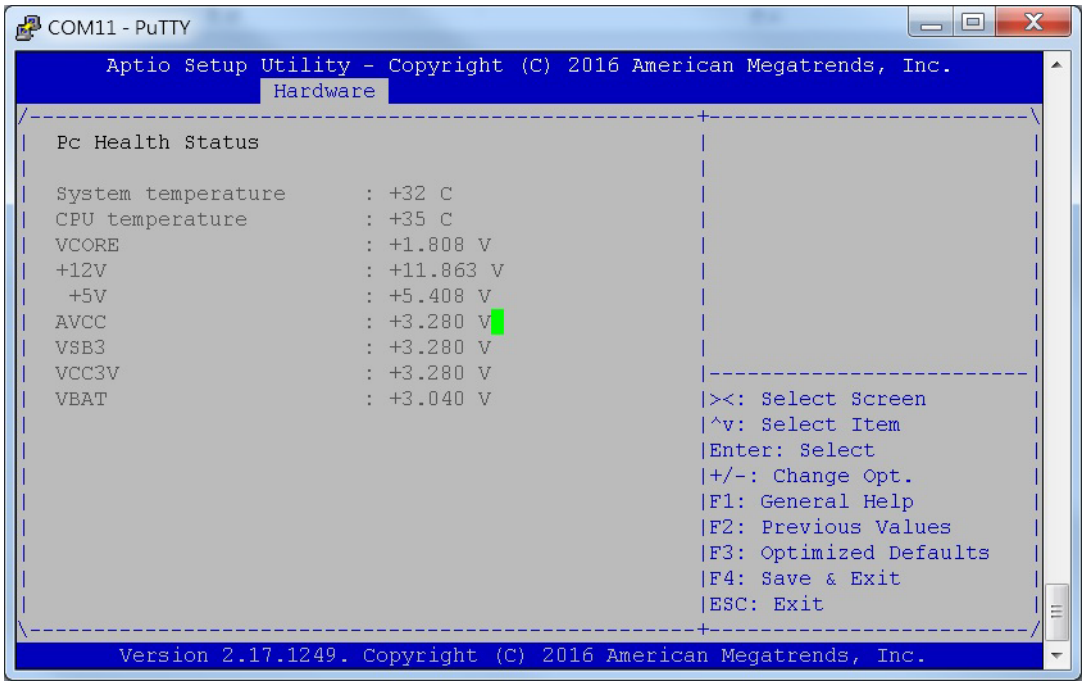


Figure 2.22 NCT6106D HW monitor screen

2.2.4 Server Management Setup

The server management setup menu features BMC-related items, such as the OS Watchdog Timer. To obtain details of the BMC self-test log and system event log, users can enable the function to record logs. Alternatively users can erase logs via the BMC self-test log submenu or the system event log submenu.

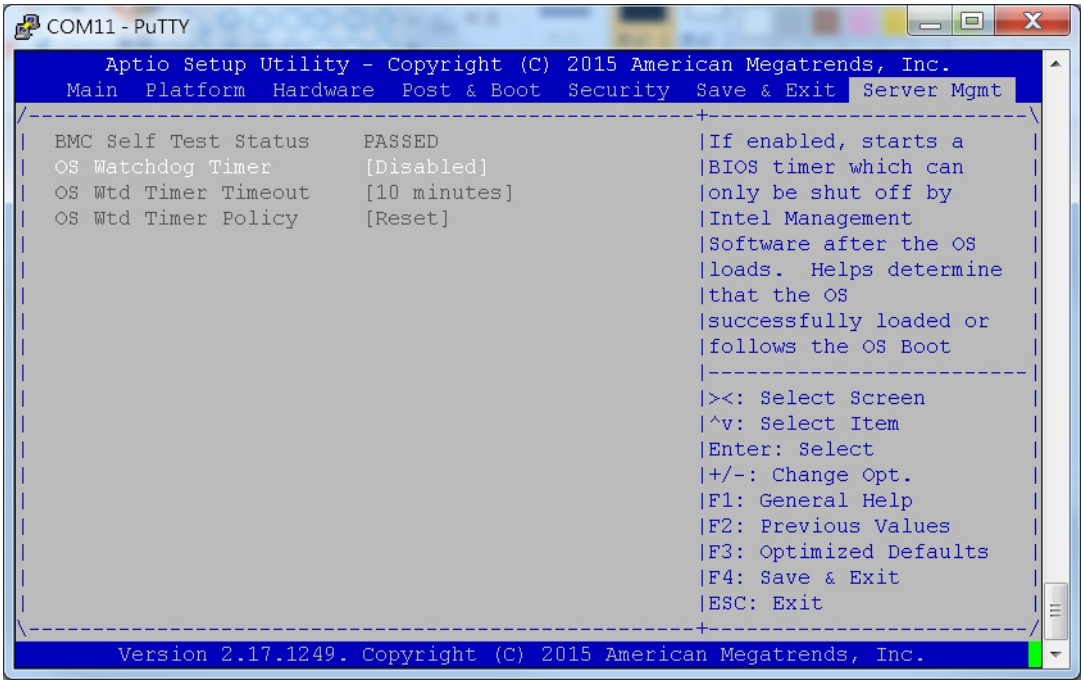


Figure 2.23 Server management configuration screen

2.2.5 Boot Setup

The Post and Boot menu allows users to configure POST behavior and boot options.

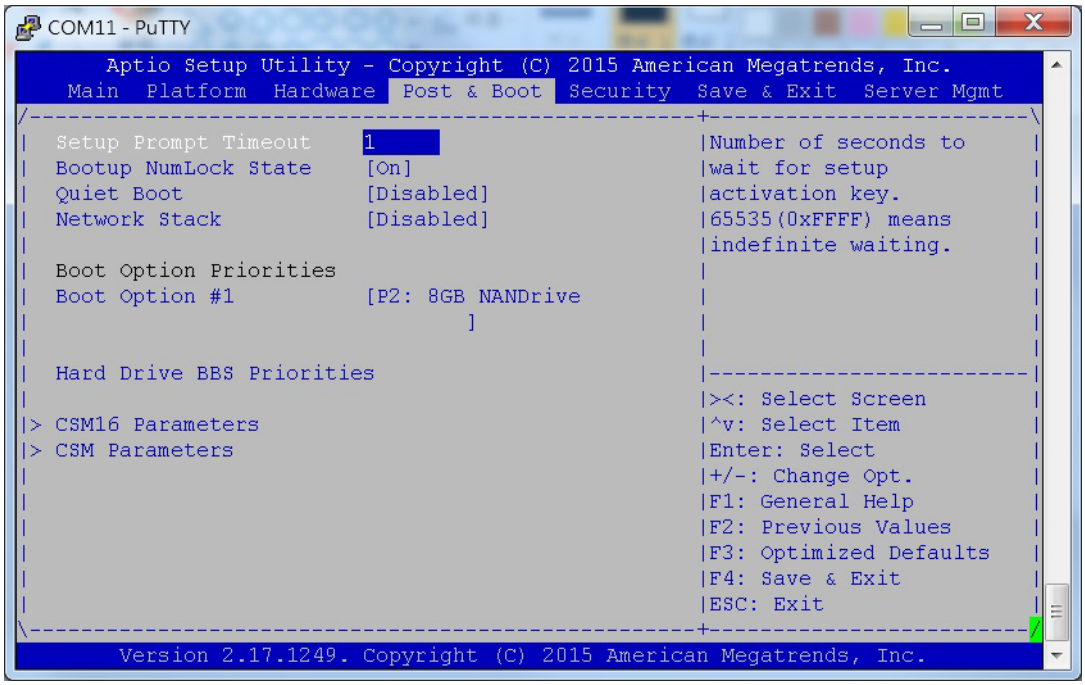


Figure 2.24 Boot configuration screen

Table 2.16: Boot Configuration

Item	Options	Description	Help Text
Setup Prompt Timeout	1 to 65535 1	Number of seconds to wait for the setup activation key. 65535(0xFFFF) means wait indefinitely.	Number of seconds to wait for the setup activation key. 65535(0xFFFF) means wait indefinitely.
Bootup NumLock State	On Off	Select the keyboard NumLock state.	Select the keyboard NumLock state.
Quiet Boot	Disabled Enabled	If enabled, POST messages are not displayed on the console. This may speed up booting. If disabled, POS messages are displayed on console.	Enable or disable quiet boot option.
Network Stack	Disabled Enabled	Enable or disable the UEFI network stack.	Enable or disable the UEFI network stack.
Boot Option #1 to #N	Type: Boot device	Specifies the priority of the available boot sources. The list includes USB flash, SAS hard drive, SATA hard drive, and UEFI network PXE. Other supported devices can be dynamically added to the list.	Specifies the priority of the available boot sources.

Drive types appear in the boot device priority menu even if no drives are present (i.e., the drives are not yet connected).

The Boot Device Priority submenu (boot sources) and “xxx Boot Device” submenus are always available even when no device is present in the corresponding boot device submenu.

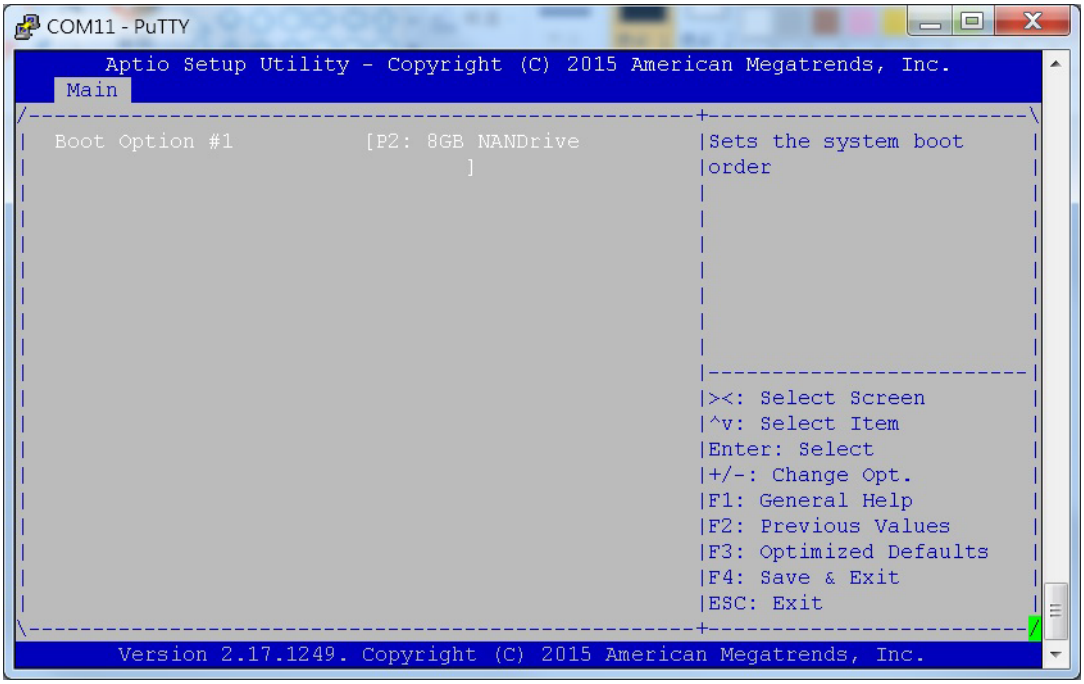


Figure 2.25 Hard disk driver BBS priorities screen

Table 2.17: Hard Disk Driver BBS Priority Settings

Item	Options	Description	Help Text
Boot Option #N	N/A	Specifies the boot priority for the available devices.	Sets the system boot order.

2.2.5.1 CSM16 Parameters

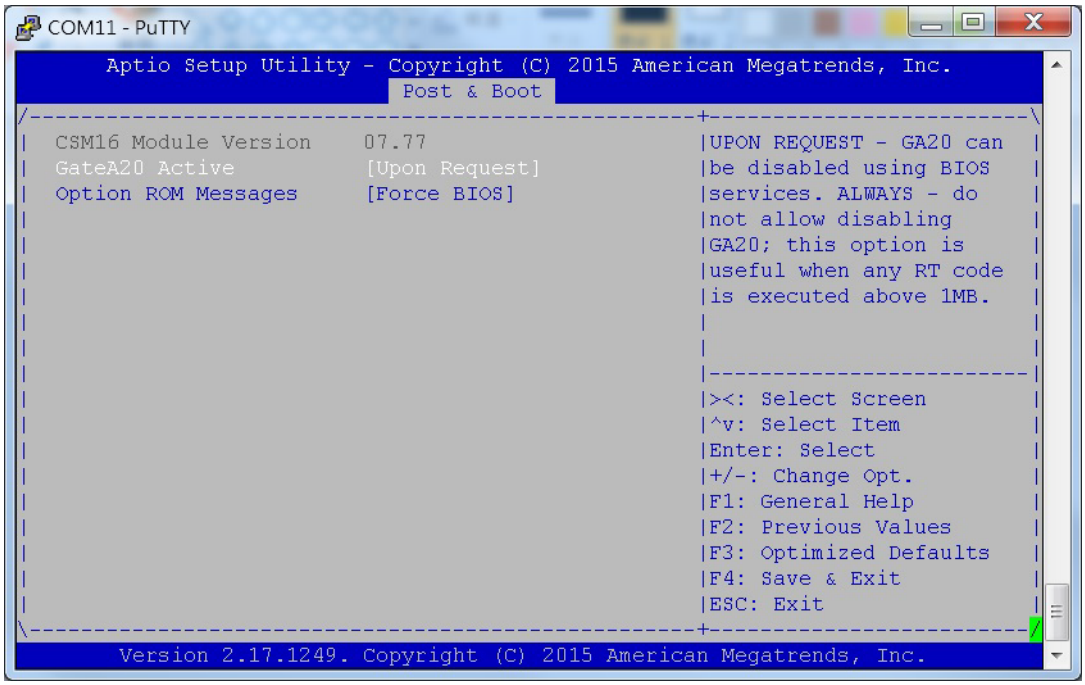


Figure 2.26 CSM16 parameters screen

Table 2.18: CSM16 Parameters

Item	Options	Description	Help Text
GateA20 Active	Upon Request Always	Enable or disable the addressing bus from receiving messages from the A20 line.	This item is useful when RT code is executed above 1MB. When this is set as "Upon Request", GA20 can be disabled using BIOS services. When it's set as "Always", it does not allow disabling GA20.
Option ROM Messages	Force BIOS Keep Current	Sets the display mode for the option ROM.	Sets the display mode for option ROM.

2.2.5.2 CSM Parameters

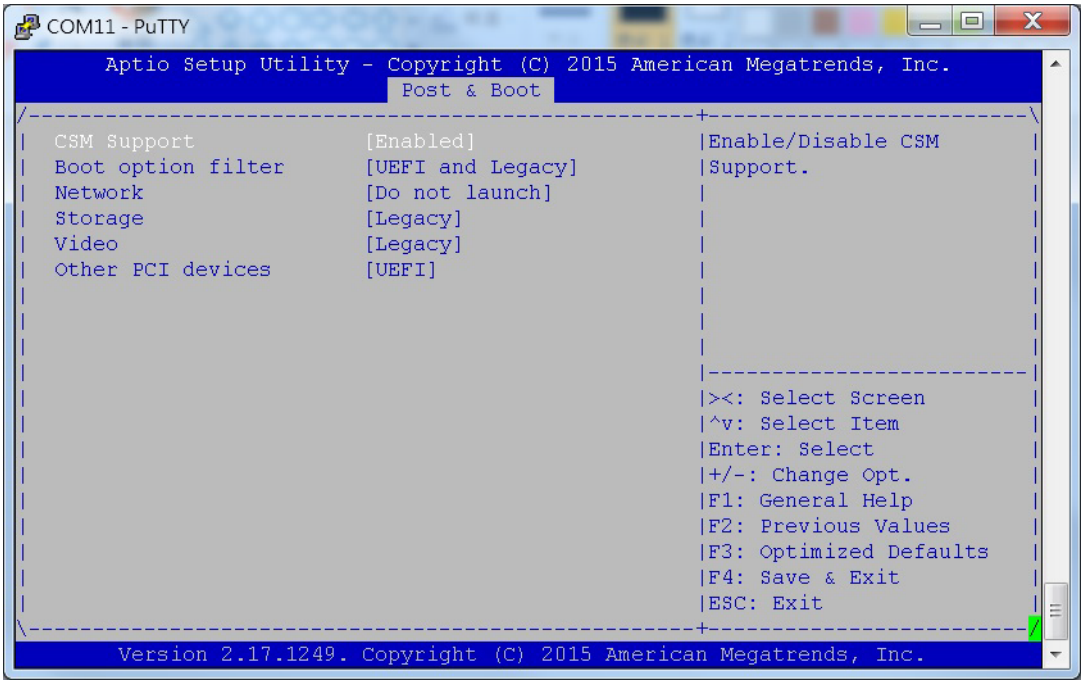


Figure 2.27 CSM parameters screen

Table 2.19: CSM Parameters

Item	Options	Description	Help Text
CSM Support	Disabled Enabled	Enable or disable CSM support.	Enable or disable CSM support.
Boot Option Filter	UEFI and Legacy UEFI only Legacy only	This option controls legacy/UEFI ROM priority.	This option controls legacy/UEFI ROM priority.
Network	Do not launch UEFI Legacy	Controls the execution of UEFI and legacy PXE OpROM.	Controls the execution of UEFI and legacy PXE OpROM.
Storage	Do not launch UEFI Legacy	Controls the execution of UEFI and legacy storage OpROM.	Controls the execution of UEFI and legacy storage PXE OpROM.
Video	Do not launch UEFI Legacy	Controls the execution of UEFI and legacy video OpROM.	Controls the execution of UEFI and legacy video OpROM.
Other PCI devices	UEFI Legacy	Sets the OpROM execution policy for devices other than Network, Storage, or Video.	Sets the OpROM execution policy for devices other than Network, Storage, or Video.

2.2.6 Security Setup

The Security page items allow users to enable password protection and set access passwords. Two password levels are provided: Administrator and User. When logging in at Administrator level, all configuration parameters can be modified. At the User privilege level, certain parameters cannot be changed and certain actions cannot be performed, as specified below.

- Modify critical platform parameters
- Disable password support
- Modify the administrator password

Those options are presented in grey text and are non-selectable and read-only at the User privilege level.

If the Administrator password feature is enabled, the BIOS will prompt users for a password before entering the setup menu. If the User password feature is enabled, the BIOS will prompt users for a password before entering the setup menu and the OS. If password protection is disabled, all users will have administrator rights.

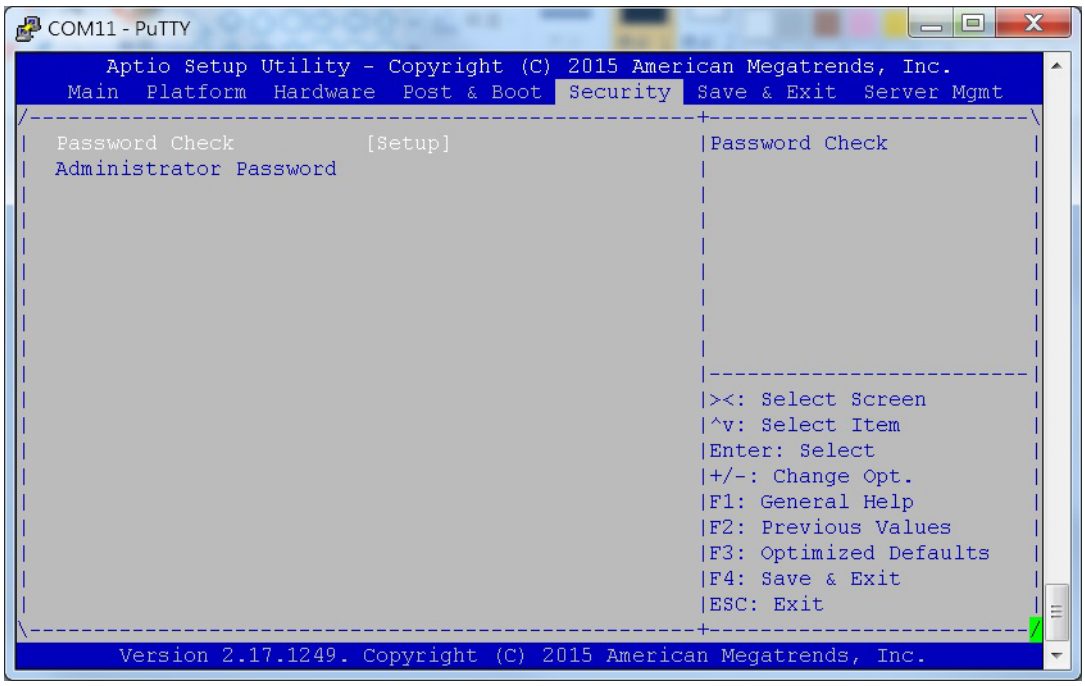


Figure 2.28 Security configuration screen

2.2.7 Save & Exit Options

The Save & Exit page provides various options for exiting the setup menu and restoring the default values for all configuration parameters.

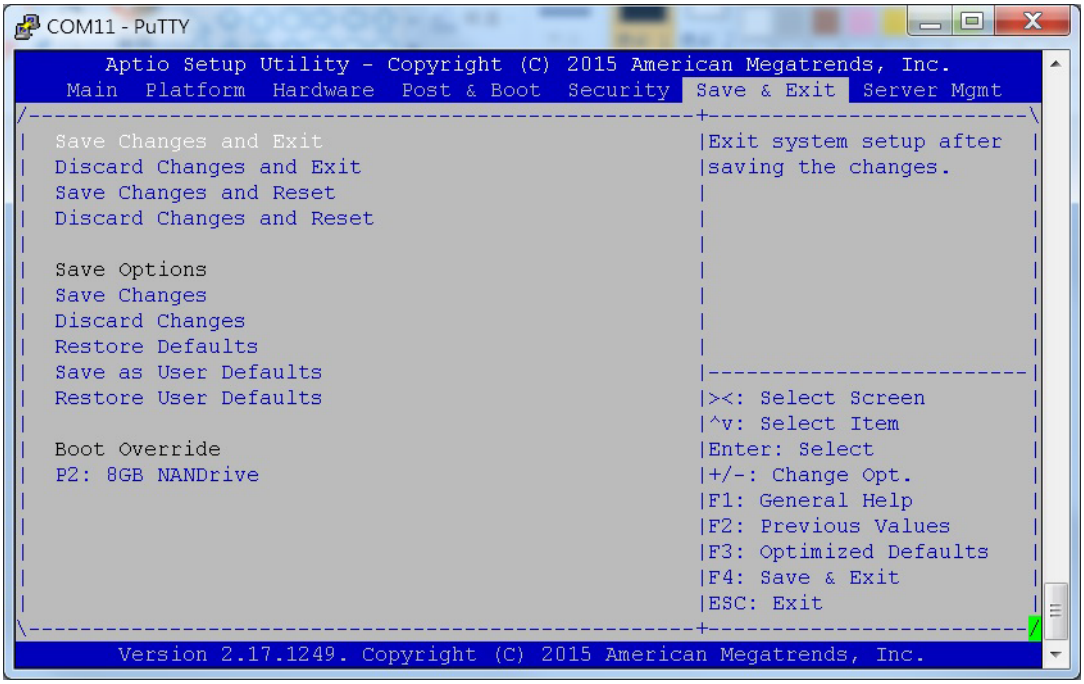


Figure 2.29 Save & Exit configuration screen

Table 2.20: Save & Exit Configuration

Item	Options	Description	Help Text
Save Changes and Exit	N/A	Save modified settings into non-volatile memory and reboot the system if necessary.	Exit system setup after saving changes.
Discard Changes and Exit	N/A	Discard modified settings, exit setup, and continue system boot up using the previous settings.	Exit system setup without saving changes.
Save Changes and Reset	N/A	Save modified settings into non-volatile memory and reboot the system.	Reset the system after saving changes.
Discard Changes and Reset	N/A	Discard modified settings, revert to the state when setup was entered, and reboot the system using the previous settings.	Reset the system without saving changes.
Save Changes	N/A	Save all changes to the setup options.	Save all changes to the setup options.
Discard Changes	N/A	Discard all changes to the setup options and revert to the settings when setup was entered.	Discard all changes to the setup options.

Table 2.20: Save & Exit Configuration			
Restore Defaults	N/A	Load the factory default settings.	Restore/load the default settings for all setup options.
Save as User Defaults	N/A	Save all changes as user defaults.	Save all changes as user defaults.
Restore User Defaults BIOS	N/A	Restore the setup options to the settings defined as user defaults.	Restore the user defaults to all setup options.

Chapter 3

BMC Firmware Operation

This chapter describes the BMC firmware features.

3.1 Module Management

The IPMI Baseboard Management Controller (BMC) located on MIC-6314 acts as a standard IPMI management controller and is an essential part of the board. The BMC's primary tasks are to ensure module health (monitoring the voltage and temperature sensors), facilitate payload state management and information data storage, and provide IPMI communication interfaces.

3.2 IPMI Interfaces

MIC-6314 provides three main IPMI messaging interfaces for connecting to the modules BMC, specifically, the local IPMB bus (IPMB) for basic communication with other modules in the chassis, the LAN side band interface (RMCP/RMCP+), and the onboard payload interface to x86 (KCS).

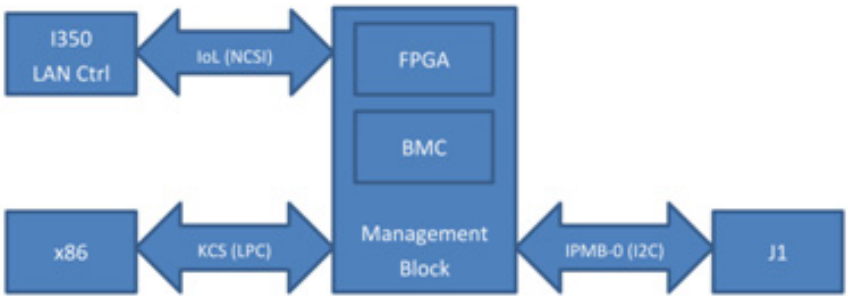


Figure 3.1 IPMI interfaces

3.2.1 IPMB

The basic IPMI connection of a BMC is the I2C-based, serial IPMB interface routed to the backplane connector. Once plugged into a backplane and supplied with power, the BMC discovers the slot connector's geographic address (GA). The GA is used to assign a unique IPMB address according to the slot number. With this IPMB address, the BMC is able to communicate with other components in the chassis.

The open source IPMItool can be used to access the BMC via IPMB.

3.2.2 KCS

The Keyboard Controller Style (KCS) protocol is used as IPMI system interface connection to the x86 part on MIC-6314. Based on the low pin count (LPC) bus, the KCS protocol is used as the local BMC interface to the BIOS and board OS. KCS is a fast IPMI interface compared to IPMB, but requires an active payload.

IPMI driver support is required to facilitate IPMItool operation from the OS level via the KCS BMC interface (see Appendix G - Driver and Tools for further information). With a working IPMI driver, the BMC can be easily accessed from the OS via KCS. No interface parameters are required to use the local onboard IPMI connection:

```
ipmitool <Command>
```

3.2.3 LAN

The IPMI LAN interface on MIC-6314 is achieved using a shared LAN controller with the x86 system. In addition to the system's PCI-Express link, a LAN controller sideband interface (Network Controller Sideband Interface [NC-SI]) is connected to the BMC. This NC-SI channel is used by the BMC to receive and transmit IPMI management traffic to the network via the LAN controller.

IPMI over LAN (IOL) uses the Remote Management Control Protocol (RMCP, specified in IPMI v1.5) in the request-response pattern for IPMI communication. IPMI v1.5 LAN messages are encapsulated in RMCP packets, while the IPMI v2.0 specification adds an enhanced protocol (RMCP+) for transferring IPMI messages and other types of payloads. RMCP+ uses the RMCP overall packet format, but defines extensions, such as encryption and the ability to carry additional traffic types (e.g., serial data), in addition to IPMI messages (refer to Section 3.11 - Serial over LAN Setup).

All of the four backplane ports of MIC-6314's Ethernet interfaces can be used for IPMI over LAN. The RJ45 LAN connectors on the front panel cannot be used for IPMI over LAN because no NCSI is connected.

Note! *The LAN controller used for IPMI communication is connected to a certain power domain related to the front handle. Thus, the handle must be closed to enable IPMI over LAN.*

The following IPMItool parameters are required for connecting to the BMC vial LAN:

```
ipmitool -I lan -H <BMC IP-Address> -U <User> -P <Password>
<Command>
```

Command Line Syntax	
-I lan	Specifies the Ethernet interface
-H <IP-Address>	IP address assigned to the BMC
-U <User>	User account, default "administrator"
-P <Password>	Password used with specified user account (default password for administrator access is "advantech")

3.3 Sensors

The MIC-6314 BMC's main task is to monitor the board voltages and temperatures. All important voltages and temperatures are connected to the BMC sensor.

The BMC management subsystem also monitors the following logical sensors:

- BMC Watchdog sensor
- FW Progress sensor
- Version change sensor
- Processor sensors (processor hot, thermal trip, etc.)
- Advantech OEM sensor: integrity sensor

3.3.1 Sensor List

All sensors provided on the MIC-6314 board are listed in the table below (including the FRU device locator record):

Table 3.1: Sensor List

No.	Sensor ID	Sensor Type (Event/Reading Type)	Description
0	MIC-6314	-	IPMI FRU Device Locator
1	BMC_WATCHDOG	Watchdog 2 (Discrete)	IPMI BMC Watchdog sensor
2	FW_PROGRESS	System Firmware Progress (Discrete)	IPMI FW Progress sensor
3	VERSION_CHANGE	Version Change (Discrete)	IPMI Version Change sensor
4	PROC_VR_HOT	OEM (Discrete)	Advantech OEM Processor HOT status
5	THERM_TRIP	OEM (Discrete)	Advantech OEM CPU Thermal Trip
6	INTEGRITY	OEM (Discrete)	Advantech OEM Integrity sensor
7	PAY_12_0-VOL	Voltage (Threshold)	Payload Power voltage 12V
8	HP_12_0-VOL	Voltage (Threshold)	12V.0 on the VPX Connector
9	PAY_5_0-VOL	Voltage (Threshold)	Payload Power voltage 5V
10	HP_5_0-VOL	Voltage (Threshold)	5V.0 on the VPX Connector
11	PAY_3_3-VOL	Voltage (Threshold)	Payload Power voltage 3.3V
12	SB_3_3-VOL	Voltage (Threshold)	Standby Power voltage 12V
13	MAN_3_3-VOL	Voltage (Threshold)	Management Power voltage 3.3V
14	BAT_3_0-VOL	Voltage (Threshold)	RTC voltage
15	CPU_CORE_1_8-VOL	Voltage (Threshold)	CPU Core voltage
16	PCH_1_5-VOL	Voltage (Threshold)	PCH voltage 1.5V
17	DDR3_1_35-VOL	Voltage (Threshold)	DDR3 voltage 1.35V
18	PCH_0_9-VOL	Voltage (Threshold)	PCH voltage 0.9V
19	CPU-TMP	Temperature (Threshold)	CPU Temperature (PECI)
20	HDD-TMP	Temperature (Threshold)	HDD Temperature
21	SYS-TMP	Temperature (Threshold)	System temperature
22	LAN_BI-TMP	Temperature (Threshold)	I350 LAN controller temperature

3.3.2 Threshold-Based Sensors

According to the IPMI specification, sensor event thresholds are classified as Non-Critical, Critical, or Non-Recoverable. When various thresholds are reached, different actions may be executed by the carrier or shelf manager (e.g., fan speed adjustment for temperature sensor events). The table below lists the six thresholds specified for the threshold-based sensors described in the following sections.

Table 3.2: Threshold Descriptions

Threshold	Description
UNR	Upper Non-Recoverable
UC	Upper Critical
UNC	Upper Non-Critical
LNC	Lower Non-Critical
LC	Lower Critical
LNR	Lower Non-Recoverable

3.3.2.1 Voltage Sensors

All voltages listed in the table below are monitored by the BMC and can be read via IPMI.

Table 3.3: Voltage Sensor List

Sensor Name	Nominal Value	LNR	LCR	LNC	UNC	UCR	UNR
PAY_12_0-VOL	12	na	10.2	na	na	13.2	na
HP_12_0-VOL	12	na	10.2	na	na	13.2	na
PAY_5_0-VOL	5	na	4.5	na	na	5.5	na
HP_5_0-VOL	5	na	4.5	na	na	5.5	na
PAY_3_3-VOL	3.3	na	3	na	na	3.6	na
SB_3_3-VOL	3.3	na	3	na	na	3.6	na
MAN_3_3-VOL	3.3	na	3	na	na	3.6	na
BAT_3_0-VOL	3	na	2.4	na	na	3.6	na
CPU_CORE_1_8-VOL	1.8	na	1.71	na	na	1.89	na
PCH_1_5-VOL	1.5	na	1.35	na	na	1.65	na
DDR3_1_35-VOL	1.35	na	1.2	na	na	1.496	na
PCH_0_9-VOL	0.9	na	0.8	na	na	1.1	na

3.3.2.2 Temperature Sensors

MIC-6314 supports temperature sensors via either board-populated ICs (e.g., TMP75) or readings from the CPU/chipset interfaces (PECI/SMBus).

Table 3.4: Temperature Sensor List

Sensor Name	Value	LNR	LCR	LNC	UNC	UCR	UNR
CPU-TMP	40	na	na	na	95	105	na
HDD-TMP	40	na	na	na	75	85	95
SYS-TMP	40	na	na	na	75	85	95
LAN_BI-TMP	40	na	na	na	90	100	110

3.3.3 Discrete Sensors

3.3.3.1 BMC Device Locator

Every BMC provides a PICMG compliant FRU device locator for the subsystem. This record is used to maintain the BMC location and type information.

3.3.3.2 BMC Watchdog Sensor

The BMC Watchdog sensor is supported according to the Watchdog 2 sensor type listed in the IPMI specification.

3.3.3.3 FW Progress Sensor

The BMC SDR contains a FW Progress sensor for logging the OS boot process. The BMC supports adding and forwarding of SEL entries from the BIOS/OS system firmware progress events by sending “Add SEL entry” commands with the matching sensor type to the BMC through the KCS interface.

3.3.3.4 Version Change Sensor

The Version Change sensor is supported according to the IPMI specification.

3.3.3.5 VR HOT Sensor

The BMC SDR is equipped with a discrete OEM sensor for monitoring the state of the CPU voltage regulator (VR HOT). The underlying bitmasks for identifying single processor voltage regulator hot events are shown in the table below.

Table 3.5: Voltage Regulator Hot Sensor Bits

Bit	7	6	5	4	3	2	1	0
Description	-	-	-	-	-	-	-	VR CPU 0 HOT

3.3.3.6 PROC HOT Sensor

The BMC features a sensor for monitoring the state of the CPU processor hot signals on each subsystem. The sensor is implemented as a discrete OEM sensor and the underlying bitmask are shown in the table below.

Table 3.6: Processor Hot Sensor Bits

Bit	7	6	5	4	3	2	1	0
Description	-	-	-	-	-	-	-	PROC HOT CPU 0

3.3.3.7 Thermal Trip Sensor

To monitor the CPU thermal trip states via the FPGA, the BMC features a discrete OEM sensor. The underlying bitmasks for identifying these events are shown in the table below.

Table 3.7: Thermal Trip Sensor Bits

Bit	7	6	5	4	3	2	1	0
Description	-	-	-	-	-	-	-	Therm Trip CPU 0

3.3.4 Example Sensor Data

The examples provided below show MIC-6314 sensor data read using the open source IPMItool.

```
[root@localhost ~]# ipmitool sdr list
BMC_WATCHDOG     | 0x00              | ok
FW_PROGRESS      | 0x00              | ok
VERSION_CHANGE   | 0x00              | ok
PROC_VR_HOT      | 0x00              | ok
THERM_TRIP       | 0x00              | ok
INTEGRITY        | 0x00              | ok
PAY_12_0-VOL     | 12.21 Volts       | ok
HP_12_0-VOL      | 12.06 Volts       | ok
PAY_5_0-VOL      | 4.94 Volts        | ok
HP_5_0-VOL       | 4.94 Volts        | ok
PAY_3_3-VOL      | 3.28 Volts        | ok
SB_3_3-VOL       | 3.33 Volts        | ok
MAN_3_3-VOL      | 3.30 Volts        | ok
BAT_3_0-VOL      | 3.04 Volts        | ok
CPU_CORE_1_8-VOL | 1.73 Volts        | ok
PCH_1_5-VOL      | 1.49 Volts        | ok
DDR3_1_35-VOL    | 1.34 Volts        | ok
PCH_0_9-VOL      | 0.90 Volts        | ok
CPU-TMP          | 38 degrees C      | ok
HDD-TMP          | 35 degrees C      | ok
SYS-TMP          | 29 degrees C      | ok
LAN_BI-TMP       | 39 degrees C      | ok
```

```
[root@localhost ~]# ipmitool sdr elist all
MIC-6314          | 00h | ok  | 160.96 | Dynamic MC @ 8Eh
BMC_WATCHDOG      | 01h | ok  | 160.96 |
FW_PROGRESS       | 02h | ok  | 160.96 |
VERSION_CHANGE    | 03h | ok  | 160.96 |
PROC_VR_HOT       | 04h | ok  |  3.96 |
THERM_TRIP        | 05h | ok  |  3.96 |
INTEGRITY         | 06h | ok  | 160.96 |
PAY_12_0-VOL      | 07h | ok  | 160.96 | 12.21 Volts
HP_12_0-VOL       | 08h | ok  | 160.96 | 12.14 Volts
PAY_5_0-VOL       | 09h | ok  | 160.96 | 4.94 Volts
HP_5_0-VOL        | 0Ah | ok  | 160.96 | 4.94 Volts
PAY_3_3-VOL       | 0Bh | ok  | 160.96 | 3.28 Volts
SB_3_3-VOL        | 0Ch | ok  | 160.96 | 3.33 Volts
MAN_3_3-VOL       | 0Dh | ok  | 160.96 | 3.28 Volts
BAT_3_0-VOL       | 0Eh | ok  | 160.96 | 3.04 Volts
CPU_CORE_1_8-VOL  | 10h | ok  |  3.96 | 1.73 Volts
PCH_1_5-VOL       | 11h | ok  | 160.96 | 1.49 Volts
DDR3_1_35-VOL     | 12h | ok  | 160.96 | 1.34 Volts
PCH_0_9-VOL       | 14h | ok  | 160.96 | 0.90 Volts
CPU-TMP           | 15h | ok  |  3.96 | 38 degrees C
HDD-TMP           | 16h | ok  | 160.96 | 35 degrees C
SYS-TMP           | 17h | ok  | 160.96 | 29 degrees C
LAN_BI-TMP        | 18h | ok  | 160.96 | 39 degrees C
```

3.3.5 Integrity Sensor

3.3.5.1 Overview

The Advantech integrity sensor is an OEM sensor that accords with the sensor data record (SDR) definition in the IPMI specification. The main purpose of the integrity sensor is to monitor internal firmware states and report events that would otherwise go unnoticed to the operator (hence “integrity sensor”).

Examples of such events include checksum errors, firmware update success/failures, and firmware rollbacks.

3.3.5.2 Sensor Characteristics

The integrity sensor does not support sensor reading and only generates event messages. These events are stored in the local system event log (SEL) and sent to the default event receiver.

The event message contains three bytes of event data. The first byte defines how the event is supposed to be treated: the value of 0xA0 defines that event data 2 and 3 contain OEM data (please reference the IPMI specification for details regarding OEM sensors).

Event data 2 is used to identify the component that the event relates to. This can be either a HPM.1 component, a logical component/feature on the board (for example FRU, RTC) or simply a board-specific event.

Event data 3 [7..3] identifies the action or a subcomponent. For example, if the component in byte 2 was a HPM.1 component, this data may report whether the event was an update, rollback, or boot failure. If the component in byte 2 was “FRU”, the data may indicate the subcomponent = area within the FRU that the event relates to.

Event data 3 [2..0] holds the result code. For the HPM.1 example above, the data may report that an update or rollback succeeded or failed. For the FRU example, the data may indicate a checksum error.

3.3.5.3 Event Data Byte Definition

The integrity sensor event byte definitions are listed in the table below.

Table 3.8: Integrity Sensor Event Definitions

Data Byte	[Bit]	Description	Value	Event Data
1	[7:0]	IPMI Header	0xA0	Event data 2 and event data 3 used as OEM data
2	[7:0]	Component	0x00 – 0x07 0x08 – 0xFE 0xFF	HPM.1 component (FW, FPGA, BIOS…) Logical component (FRU, RTC…) Board-specific event
3	[7:3]	Action/Subcomponent	b00000 b00001 b00010 b00011 b00100 b00101 b00110 b00111 b01000 b01001 b01010 b01011 b01100 b01101 b01110 b01111… …b11111	Update Recovery/Rollback Manual Rollback Automatic Rollback Activation Flash 0 Boot Flash 1 Boot Common Header Internal Area Chassis Info Area Board Info Area Product Info Area Multi Record Area Time Synchronization Graceful Shutdown Not defined yet… Not defined yet
3	[2:0]	Result	b000 b001 b010 b011 b100 b101 b110 b111	Successful Failed Aborted Checksum Error Timeout Initiated Finished Unspecified Error

3.3.5.4 Event Data Translation

The structured definition allows for simple translation of each integrity sensor event message. An example integrity sensor SEL event (0x0A0100) is shown below. The three event data bytes could be translated in following manner:

Data 1: 0x0A: Header

Data 2: 0x01: Logical component (BMC FW)

Data 3: 0x00: b 0 0 0 0 0 0 0 0

Update Successful

This example integrity sensor event reports a successful BMC firmware update.

3.3.5.5 Event Data Table

All event data combinations supported by the BMC integrity sensor are listed in the table below.

Table 3.9: Integrity Sensor Event Data

Component	Action / Subcomponent	Result	Byte 1	Byte2
BMC FW	Update	Successful	0x01	0x00
	Update	Timeout	0x01	0x04
	Update	Aborted	0x01	0x02
	Activation	Failed	0x01	0x21
	Manual Rollback	Initiated	0x01	0x15
	Automatic Rollback	Initiated	0x01	0x1D
	Rollback	Finished	0x01	0x10
	Rollback	Failed	0x01	0x09
	Graceful Shutdown	Timeout	0x01	0x74
FPGA	Update	Successful	0x02	0x00
	Update	Timeout	0x02	0x04
	Update	Aborted	0x02	0x02
	Recovery	Finished	0x02	0x10
BIOS	Update	Successful	0x03	0x00
	Update	Timeout	0x03	0x04
	Update	Aborted	0x03	0x02
	Flash 0 Boot	Failed	0x03	0x29
	Flash 1 Boot	Failed	0x03	0x31

3.3.5.6 Example Event Identification

The integrity sensor is listed as the last MIC-6314 sensor (see the example below read using the IPMItool).

```
[root@localhost ~]# ipmitool sdr elist
…
INTEGRITY        | 06h | ok  | 160.96 |
```

As previously stated, the integrity sensor does not provide a sensor reading (disabled), but does support event generation at any time.

Occurred events are stored as records in the system event log and can be read using the following IPMItool command:

```
[root@localhost ~]# ipmitool sel elist
…
684 | 07/15/2016 | 18:49:19 | OEM INTEGRITY | OEM Specific |
Asserted
…
```

Detailed information regarding single system events (event data bytes) in the SEL can be displayed using the IPMItool “sel get <entry>”.

```
[root@localhost ~]# ipmitool sel get 0x684
SEL Record ID          : 0684
 Record Type           : 02
 Timestamp             : 07/15/2016 18:49:19
 Generator ID          : 008e
 EvM Revision          : 04
 Sensor Type           : OEM
 Sensor Number         : 06
 Event Type            : Sensor-specific Discrete
 Event Direction       : Assertion Event
 Event Data (RAW)      : a00335
 Event Interpretation  : Missing
 Description           : OEM Specific

Sensor ID              : INTEGRITY (0x6)
 Entity ID             : 160.96
 Sensor Type (Discrete): Unknown (0xC0)
[root@localhost ~]# ipmitool sel get 0x684
SEL Record ID          : 0684
 Record Type           : 02
 Timestamp             : 07/15/2016 18:49:19
 Generator ID          : 008e
 EvM Revision          : 04
 Sensor Type           : OEM
 Sensor Number         : 06
 Event Type            : Sensor-specific Discrete
 Event Direction       : Assertion Event
 Event Data (RAW)      : a00335
 Event Interpretation  : Missing
 Description           : OEM Specific

Sensor ID              : INTEGRITY (0x6)
 Entity ID             : 160.96
 Sensor Type (Discrete): Unknown (0xC0)
[root@localhost ~]# ipmitool sel get 0x684
SEL Record ID          : 0684
 Record Type           : 02
 Timestamp             : 07/15/2016 18:49:19
 Generator ID          : 008e
 EvM Revision          : 04
 Sensor Type           : OEM
 Sensor Number         : 06
 Event Type            : Sensor-specific Discrete
 Event Direction       : Assertion Event
 Event Data (RAW)      : a00335
 Event Interpretation  : Missing
 Description           : OEM Specific

Sensor ID              : INTEGRITY (0x6)
 Entity ID             : 160.96
 Sensor Type (Discrete): Unknown (0xC0)
```

The “Event Data” field reflects the three bytes required to identify the integrity sensor event that occurred.

3.4 FRU Information

The BMC provides IPMI-defined field-replaceable unit (FRU) information about the board. The MIC-6314 FRU data includes general board data, such as the product name, hardware version, and serial number. A total of 2 Kb of non-volatile storage space is reserved for FRU data. The board's IPMI FRU information is accessible via any BMC interface and can be retrieved at any time.

3.4.1 FRU Information Access Commands

The FRU device IPMI commands are supported by the BMC to enable reading and writing of board FRU information. Correct and board-specific FRU data is programmed into every module in the factory. Please be careful when using the standard IPMI FRU write command (avoid use if possible). Incorrect FRU data can destroy the payload functionality!

3.4.2 Example FRU Data

An example excerpt of default MIC-6314 FRU data (board and product information areas) read using the Linux IPMItool is shown below.

```
[root@localhost ~]# ipmitool fru
FRU Device Description : Builtin FRU Device (ID 0)
 Board Mfg Date        : Mon Jan  1 00:00:00 1996
 Board Mfg             : Advantech
 Board Product         : MIC-6314
 Board Serial          : AKA1234567
 Board Part Number     : MIC-6314
 Product Manufacturer  : Advantech
 Product Name          : MIC-6314
 Product Part Number   : MIC-6314
 Product Version       : A1 02
 Product Serial        : AKA1234567
```

3.5 OEM Commands

Advantech's management solutions support extended OEM IPMI command sets based on the IPMI-defined OEM/Group network function (NetFn) codes 2Eh/2Fh.

The first three data bytes of IPMI requests and responses under the OEM/Group network function identify the OEM vendor that specified the command functionality. More precisely, the vendor IANA Enterprise Number for the defining body occupies the first three data bytes in a request, and the first three data bytes following the completion code position in a response. Advantech's IANA Enterprise Number used for OEM commands is 002839h.

The MIC-6314 BMC supports the following Advantech IPMI OEM commands:

Table 3.10: OEM Command Overview

Command	LUN	NetFn	CMD
Store Configuration Settings	00h	2Eh	40h
Read Configuration Settings	00h	2Eh	41h
Read Port 80 (BIOS POST Code)	00h	2Eh	80h
Read MAC Address	00h	2Eh	E2h
Load Default Configuration	00h	2Eh	F2h

3.5.1 IPMItool Raw Command

To use Advantech OEM commands with the open source IPMItool, users must employ the “raw” command of IPMItool. The structure of the IPMItool raw command is detailed below.

General raw request:

```
ipmitool raw <netfn> <cmd> [data]
```

Response, if raw <netfn> is 2Eh (OEM/Group):

```
<IANA Enterprise Number> [data]
```

3.5.2 Configuration OEM Commands

The Read and Store Configuration OEM commands can be used to read and change several important board settings. The required command details are described in the following sections.

3.5.3 LAN Controller Interface Selection

The BMC firmware provides OEM IPMI commands to allow users to switch the one BMC connected NC-SI interface between four I350 LAN channels. This command can be used to read the selected IPMI-over-LAN interface and change the selection.

LAN controller interface selection settings:

00h: Group 0, I350 Port 2 and Port 3 (BMC default)

01h: Group 1, I350 Port 0 and Port 1

Read LAN interface selection:

```
ipmitool raw 0x2e 0x41 0x39 0x28 0x00 0x04 0x00
```

Response:

```
39 28 00 <setting>
```

Change LAN interface selection:

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x04 0x00 <setting>
```

Response:

```
39 28 00
```

3.5.3.1 LAN Controller Channel Selection and Priority

In addition to the selected LAN controller interface, users may need to configure every LAN controller channel (port) as a dedicated NC-SI interface to the BMC. Additional OEM commands for configuring the NC-SI LAN controller channel selection and priority are provided to ensure flexible configuration.

LAN channel selection priority setting list:

0 = The first channel that to be linked gets the NC-SI connection to the BMC.

1 = Channel 1 is the preferred port if available, otherwise use channel 2 if available.

2 = Channel 2 is the preferred port if available, otherwise use channel 1 if available.

3 = Channel 1 is the only allowed port, always use it, never change to channel 2.

4 = Channel 2 is the only allowed port, always use it, never change to channel 1.

The NC-SI LAN controller channel setting is stored permanently (non-volatile EEPROM). The default value is 0.

Read LAN channel selection priority:

```
ipmitool raw 0x2e 0x41 0x39 0x28 0x00 0x04 0x01
```

Response:

```
39 28 00 <setting>
```

Change LAN channel selection priority:

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x04 0x01 <setting>
```

Response:

```
39 28 00
```

3.5.4 FPGA COM Port UART MUX

MIC-6314 features several serial interfaces that can be flexibly configured by implementing an UART MUX (refer to Section 3.6 – UART and UART Multiplexer). The BMC provides OEM commands for configuring UARTs via IPMI. The available COM1 and COM2 port settings are shown below (Advantech recommends that you verify the UART dependency.).

COM interfaces:

Table 3.11: OEM Interfaces

Port	Interface
0x00	COM1
0x01	COM2
0x02	BMC UART

COM1 MUX:

Table 3.12: COM1 UART MUX Settings

Setting	Connection
0x00	No interface connected, open
0x01	Serial over LAN (SOL)
0x02	Front panel RJ45
0x03	RTM 1
0x04	RTM 2

COM2 MUX:

Table 3.13: COM2 UART MUX Settings

Setting	Connection
0x00	No interface connected, open
0x01	Serial overLAN (SOL) (default)
0x02	Front panel RJ45
0x03	RTM 1
0x04	RTM 2

BMC UART MUX:

Setting	Connection
0x00	No interface connected, open
0x01	Front panel RJ45
0x02	RTM 1
0x03	RTM 2

Note! *The COM1 UART is the main interface with comparatively higher priority.*

Read COM port UART MUX setting:

```
ipmitool raw 0x2e 0x41 0x39 0x28 0x00 0x08 <port>
```

Response:

```
39 28 00 <setting>
```

Change COM port UART MUX setting:

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x08 <port> <setting>
```

Response:

```
39 28 00
```

3.5.5 BMC UART (CLI) Baud Rate OEM Command

Users can change the baud rate of the BMC UART via the COM port.

Read the BMC UART baud rate setting:

```
ipmitool raw 0x2e 0x41 0x39 0x28 0x00 0x0c 0x00
```

Response:

```
39 28 00 <setting>
```

Change the BMC UART baud rate setting:

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x0c 0x00 <setting>
```

Response:

```
39 28 00
```

Setting	Baud Rate
0x00	9600
0x01	14400
0x02	19200
0x03	38400
0x04	57600
0x05	115200

3.5.6 BMC UART (CLI) Enable/Disable OEM Command

To enable or disable BMC UART access, use the OEM command shown below, where 1 indicates enable, and 0 indicates disable.

Read the BMC UART baud rate setting:

```
ipmitool raw 0x2e 0x41 0x39 0x28 0x00 0x0c 0x01
```

Response:

```
39 28 00 <setting>
```

Change the BMC UART baud rate setting:

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x0c 0x01 <setting>
```

Response:

```
39 28 00
```

3.5.7 Read Port 80 (BIOS POST Code) OEM Command

To read the actual BIOS boot state via IPMI, the BMC provides an Advantech OEM command to reflect the actual BIOS POST (Port 80) code.

```
ipmitool raw 0x2e 0x80 0x39 0x28 0x00
```

Response:

```
39 28 00 <POST Code>
```

3.5.8 MAC Address Mirroring OEM Command

The LAN controller MAC addresses are stored in the FRU EEPROM to ensure the MACs are available even when the payload is not powered on. This helps to relate the MAC address and the physical/logical module location.

The MIC-6314 board is equipped with a total of five MAC addresses.

Table 3.14: MAC Address Mapping

MAC Number	LAN Interface
0	LAN1
1	LAN2
2	LAN3
3	LAN4
4	BMC NCSI MAC

Read MAC address OEM command:

```
ipmitool raw 0x2e 0xe2 0x39 0x28 0x00 <MAC Number>
```

Response:

```
39 28 00 <MAC-Address>
```

3.5.9 Load Default Configuration OEM Command

Several configurations settings are provided by the BMC. To reset all settings to their default values, an OEM command is available to achieve this using only one IPMI command.

```
ipmitool raw 0x2e 0xF2 0x39 0x28 0x00
```

Response:

```
39 28 00
```

3.5.10 Swap BIOS Banks OEM Command

The board features two BIOS banks, one for active BIOS and the other for redundancy. Users can swap the BIOS banks manually using the OEM command shown below. Note that the BIOS banks can only be swapped when the payload power is turned off.

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x03 0x00 0x00
```

Response:

```
39 28 00
```

3.5.11 Graceful Shutdown Timeout OEM Command

The BMC will begin a countdown after receiving a graceful shutdown request, and force the payload power to turn off after timeout. Users can access and configure the timeout settings using the OEM command shown below.

Read the graceful timeout setting:

```
ipmitool raw 0x2e 0x41 0x39 0x28 0x00 0x0e 0x01
```

Response:

```
39 28 00 <timeout>
```

Change the graceful timeout setting:

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x0e 0x01 <timeout>
```

Response:

```
39 28 00
```

3.6 UART and UART Multiplexer

3.6.1 UART Block Diagram

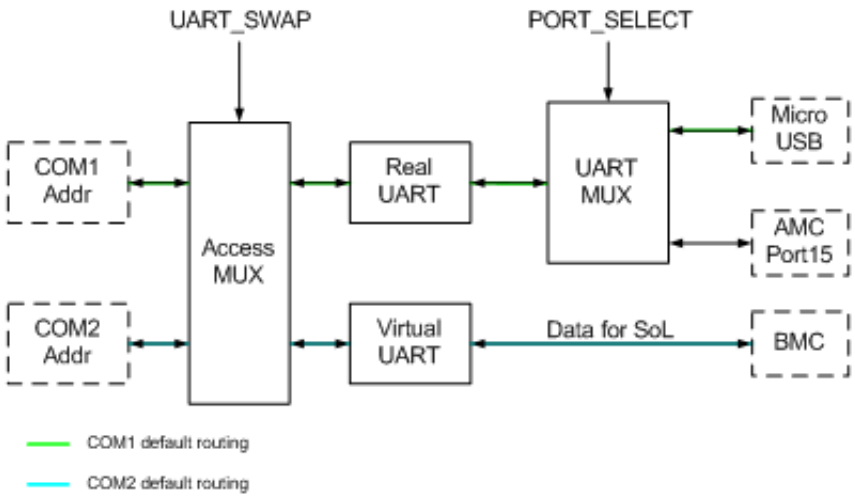


Figure 3.2 UART functional block overview

3.7 ACPI

3.7.1 ACPI-Featured Graceful Shutdown

Note! *The payload OS used with MIC-6314 must support ACPI to enable the module graceful shutdown feature.*

If a shutdown request is sent (via a hot-swap front panel handle “open” event or an IPMI command), the BMC will initiate OS shutdown via the ACPI power button signal routed to the x86 system. The ACPI daemon running on the payload OS starts to shut down the system once it detects the ACPI event. When OS shutdown is complete, the payload will indicate the achieved sleep state to the BMC.

3.7.2 Graceful Shutdown Timeout

A graceful shutdown timeout is implemented for payload operating systems without ACPI support or in the event that the shutdown process is not completed (no active x86 sleep state).

If the BMC does not receive a sleep state activated signal within before the timeout period of 60 seconds, it will still power off the payload.

3.8 BIOS Failover/Redundancy

3.8.1 Overview

MIC-6314 supports BIOS redundancy via the BMC. Two BIOS SPI flashes are provided on the board. This BIOS redundancy mechanism is responsible for managing flash failover in the event that the selected BIOS fails to boot.

This could happen if, for example, a BIOS update over HPM.1 was performed and the new BIOS version does not boot. In such an event, the BMC will revert to the BIOS version previously used.

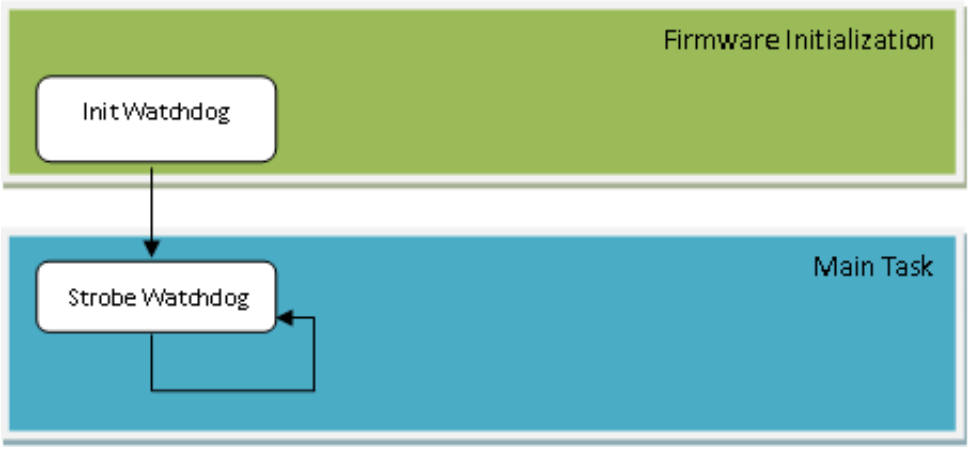
3.8.2 BIOS Boot Watchdog

The BMC is equipped with an IPMI-compliant BMC Watchdog for monitoring the BIOS boot progress. The BMC will initiate a BIOS SPI flash swap if the BMC Watchdog is triggered during BIOS execution (e.g., the selected BIOS is corrupt).

3.9 Supported Watchdogs

3.9.1 Firmware Watchdog

The Firmware Watchdog monitors BMC functionality. If the BMC hangs or stops execution, the watchdog will not be restarted. The watchdog “bites” after a timeout and resets the BMC to recover the controller from the error state.



If the watchdog is triggered, the IPMB is isolated from the controller. The payload is not affected and the FRUs operational state remains untouched.

3.9.2 BMC Watchdog

The BMC Watchdog is fully compliant with the IPMI v2.0 specification and supports the following IPMI commands:

- Reset Watchdog Timer (IPMI 2.0 specification 27.5)
- Set Watchdog Timer (IPMI 2.0 specification 27.6)
- Get Watchdog Timer (IPMI 2.0 specification 27.7)

To ensure high reliability of the MIC-6314 payload, the BMC Watchdog is enabled by default for BIOS monitoring. Additional information is provided in Section 3.8 - BIOS Failover/Redundancy.

3.10 Resets

Several reset types are support by the board. This section provides an overview of the naming and differences between the available resets.

3.10.1 Baseboard Management Controller Resets

The MIC-6314 BMC supports two resets types: cold and warm resets, according to the IPMI specification.

3.10.1.1 BMC Cold Reset

The cold BMC reset causes the default settings of all internal and external data/states (e.g., message buffers, interrupt settings, sensor and event configurations, and FRU LED states) and power up defaults to be restored.

Some events leading to BMC cold resets are outlined as follows:

- When the BMC is powered on, a cold BMC reset is performed.
- If the management power drops below a critical value, the BMC is cold reset. When the management power returns to its normal value, the BMC is brought out of reset.
- If the internal watchdog timer of the BMC expires, the BMC is cold reset.
- Users can force a BMC cold reset by pressing the front panel reset button and holding for at least five seconds.
- Software is used to execute a standard IPMI “cold reset” command.

3.10.1.2 BMC Warm Reset

The warm BMC reset is similar to the cold reset, but with additional preserved data/states (e.g., addresses and enable settings). With a warm reset, which can be executed via a standard IPMI command, the BMC firmware recovers its state from local memory.

3.10.2 Payload Reset

In addition to various management controller reset types, the board also supports payload resets. The x86 system represents the payload of the MIC-6314 board.

3.10.2.1 Payload Cold Reset

A payload cold reset means that the hardware is reset to the module payload part, similar to a power on reset. Some events that can cause payload cold resets are listed as follows:

- Payload power activation after hot swap state change.
- The front panel reset button is pressed for a short period (less than five seconds).
- The PICMG “FRU control (cold reset)” IPMI command is sent to the BMC.
- The IPMI chassis power command is sent to the BMC.
- IPMI BMC Watchdog events.
- “Control-Alt-Delete” is pressed on a connected keyboard.
- Standard operating system reset commands (e.g., Linux reboot).

3.11 Serial Over LAN Setup

Serial over LAN (SOL) is an extension to IPMI over LAN (IOL) and allows it to transmit serial data via LAN. Defined in the IPMI v2.0 specification, SOL is based on the RMCP+ protocol for encapsulating serial data in network packets and exchanging them via LAN.

With SOL, users can connect to a virtual serial console (e.g., payload x86 system) remotely. SOL can also be used on MIC-6314 for serial-based OS and pre-OS communication over LAN (e.g., via the OS command-line interface and serial redirected BIOS menu).

3.11.1 Preconditions for SOL

3.11.1.1 Supported LAN interfaces

All of MIC-6314's Ethernet interfaces to the backplane can be used for SOL.

Note! *The LAN controller used for SOL is connected to a certain power domain related to the front handle. To enable SOL use, the front handle must be closed.*

3.11.1.2 LAN Controller and UART MUX Configuration

The LAN and UART configuration is flexible and supports various configurations. To avoid incorrect configurations, users should always verify the actual LAN and UART configuration settings before working with SOL.

1. Select the LAN interface to be used (group and channel).
2. Ensure that the LAN channel priority is appropriate.
3. Select the UART interface to be used (COM1 or COM2).

3.11.1.3 Default Parameters

Following default parameters are ideal for the initial MIC-6314 LAN setup:

IP-Address: 0.0.0.0

LAN Channel Number: 5

Username: "administrator"

Password: "advantech"

3.11.2 LAN Configuration with IPMItool

The open source IPMItool utility is used for MIC-6314 SOL and LAN parameter configuration. Any utility that is based on standard IPMI commands can also be used.

To obtain an overview of all possible commands within an IPMItool command group, use the single keywords (e.g., "lan", "user", or "sol").

3.11.2.1 LAN Commands

- lan print [channel number]
  This command can be used to obtain the LAN configuration parameters for a given channel.

```
[root@localhost ~]# ipmitool lan print
Set in Progress         : Set Complete
Auth Type Support       : NONE MD5 PASSWORD
Auth Type Enable        : Callback : NONE MD5 PASSWORD
                        : User     : NONE MD5 PASSWORD
                        : Operator : NONE MD5 PASSWORD
                        : Admin    : NONE MD5 PASSWORD
                        : OEM      :
IP Address Source       : Static Address
IP Address              : 192.168.1.1
Subnet Mask             : 255.255.255.0
MAC Address             : 00:0b:ab:3e:45:87
Default Gateway IP      : 0.0.0.0
RMCP+ Cipher Suites     : 0,1,2,3,6,7,8,11,12
Cipher Suite Priv Max   : aaaaaaaaaXXXXXX
                        :     X=Cipher Suite Unused
                        :     c=CALLBACK
                        :     u=USER
                        :     o=OPERATOR
                        :     a=ADMIN
                        :     O=OEM
```

- lan set <channel> <command> [option]
  This command can be used to change several BMC LAN parameters (e.g., the IP address, netmask, and gateway IP address). The example provided below demonstrates how to change the BMC IP address.

```
[root@localhost ~]# ipmitool lan set 5 ipaddr 172.21.35.104
Setting LAN IP Address to 172.21.35.104
```

3.11.2.2 User Commands

- user list
  This command can be used to obtain a list of all supported users.

```
[root@localhost ~]# ipmitool user list
ID  Name             Callin  Link Auth  IPMI Msg   Channel Priv
Limit
1                    true    true       true       NO ACCESS
2   callback         true    true       true       NO ACCESS
3   user             true    true       true       NO ACCESS
4   operator         true    true       true       NO ACCESS
```

- user set name <user id> [username]
  This command can be used to change the user name.

```
[root@localhost ~]# ipmitool user set name 2 newuser
```

- user set password <user id> [password]
  This command can be used to change the user password.

```
[root@localhost ~]# ipmitool user set password 2 newpassword
```

3.11.3 SOL Session with IPMItool

Advantech recommends using IPMItool to successful open a SOL session with MIC-6314. The “lanplus” interface (RMCP+) of IPMItool is required to change the SOL parameters and establish SOL sessions.

The following general IPMItool parameters are required for RMCP+ and IPMItool “sol” commands:

```
ipmitool -I lanplus -H <BMC IP-Address> -U <User> -P <Pass-
word> sol <SOL-Command>
```

Command Line Syntax:	
-I lanplus	Specifies RMCP+ as the desired protocol
-H <IP-Address>	IP address assigned to the BMC
-U <User>	User account, default “administrator”
-P <Password>	Password used with the specified user account (default password for administrator access is “advantech”)

3.11.3.1 SOL Parameter Commands

- sol info [channel number]
  This command can be used to read the SOL configuration parameters for a given channel.

```
# ipmitool -I lanplus <BMC IP-Address> -U <User> -P <Password>
sol info
Set in progress                 : set-complete
Enabled                         : false
Force Encryption                : true
Force Authentication            : true
Privilege Level                 : ADMINISTRATOR
Character Accumulate Level (ms) : 250
Character Send Threshold        : 32
Retry Count                     : 2
Retry Interval (ms)             : 1000
Volatile Bit Rate (kbps)        : 115.2
Non-Volatile Bit Rate (kbps)    : 115.2
Payload Channel                 : 7 (0x07)
Payload Port                    : 623
```

- sol set <parameter> <value> [channel]
  This command can be used to modify specific SOL configuration parameters.

```
# ipmitool -I lanplus <BMC IP-Address> -U <User> -P <Password>
sol set

SOL set parameters and values:

  set-in-progress             set-complete | set-in-progress |
commit-write
  enabled                      true | false
  force-encryption             true | false
  force-authentication         true | false
  privilege-level              user | operator | admin | oem
  character-accumulate-level   <in 5 ms increments>
  character-send-threshold     N
  retry-count                  N
  retry-interval               <in 10 ms increments>
  non-volatile-bit-rate       serial | 9.6 | 19.2 | 38.4 | 57.6
| 115.2
  volatile-bit-rate           serial | 9.6 | 19.2 | 38.4 | 57.6
| 115.2
```

3.11.3.2 SOL Session Activation

The IPMItool “sol activate” command must be issued to establish the SOL to MIC-6314 session remotely.

```
# ipmitool -I lanplus <BMC IP-Address> -U <User> -P <Password>
sol activate
[SOL Session operational.  Use ~? for help]
…
~. [terminated ipmitool]
```

To terminate an active IPMItool SOL session, use the “~” + “.” (tilde and period) key sequence.

Chapter 4

HPM.1 Update

This chapter explains how to update the software/firmware components.

4.1 HPM.1 Preconditions

4.1.1 IPMItool

Before upgrading, users must prepare a HPM.1-capable update utility. Advantech recommends using the open and verified “IPMItool” (>= version 1.8.10). Generally, any tool that complies with the PICMG HPM.1 R1.0 specification can be used.

4.1.2 Interfaces

HPM.1 provides a means to upgrade firmware using various interfaces

MIC-6314 supports following IPMI interfaces:

- KCS (local payload interface, active payload, and OS support required)
- IPMB (remote, bridged via the chassis manager, independent of payload)
- LAN interface (remote, active payload required)

The upgrade procedures explained In this chapter are demonstrated using the KCS interface because it is provides the easiest method of communication.

The procedures when using a LAN or IPMB interface are roughly the same, only the required IPMItool interface parameters differ.

4.2 BMC Bootloader Upgrade

4.2.1 Load New BMC Bootloader Image

Input the IPMItool HPM.1 upgrade command and select the new BMC bootloader image.

```
[root@localhost ~]# ipmitool hpm upgrade
mic6313_bootloader_standard_0x01_
0x01_adv.img


PICMG HPM.1 Upgrade Agent 1.0.9:

Validating firmware image integrity...OK
Performing preparation stage...
Services may be affected during upgrade. Do you wish to con-
tinue? (y/n): y
OK

Performing upgrade stage:

------------------------------------------------------------
------------------
|ID  | Name            |                        Ver-
sions                                 | %   |
|    |                 |     Active      |     Backup       |
File          |     |
|----|-----------------|-----------------|-----------------|-----
------------|----|
|   0|6313 BMC         |   1.01 00000000 |   0.23 00000000  |
1.01 00000000  |100%|
|     |Upload Time: 00:20                | Image Size:  27,757
bytes                    |
------------------------------------------------------------
------------------
(*) Component requires Payload Cold Reset

Firmware upgrade procedure successful
```

4.2.2 Activate BMC Bootloader

After the new BMC bootloader is successfully downloaded to the board (known as the “deferred” version), the bootloader must be activated or the BMC reset to enable operation. Use following HPM.1 command to activate the bootloader:

```
[root@localhost ~]# ipmitool hpm activate

PICMG HPM.1 Upgrade Agent 1.0.9:

Waiting firmware activation...OK
```

4.3 BMC Firmware Upgrade

4.3.1 Load New BMC Firmware Image

Input the IPMItool HPM.1 upgrade command and select the new BMC firmware image.

```
[root@localhost ~]# ipmitool hpm upgrade
mic6313_standard_hpm_fw_01_01.img


PICMG HPM.1 Upgrade Agent 1.0.9:

Validating firmware image integrity...OK
Performing preparation stage...
Services may be affected during upgrade. Do you wish to con-
tinue? (y/n): y
OK

Performing upgrade stage:

------------------------------------------------------------
------------------
|ID  | Name           |                      Ver-
sions                              | %   |
|    |              |     Active     |     Backup       |
File         |     |
|----|-------------|-----------------|-----------------|-----
------------|----|
|   1|6313 BMC       |   1.01 00000000 |   0.23 00000000  |
1.01 00000000  |100%|
|     |Upload Time: 00:26               | Image Size:  333252
bytes                   |
------------------------------------------------------------
------------------
(*) Component requires Payload Cold Reset

Firmware upgrade procedure successful
```

4.3.2 Activate BMC Firmware

After the new BMC firmware is successfully downloaded to the board (known as the “deferred” version), it needs to be activated before it will be functional. Use following HPM.1 command:

```
[root@localhost ~]# ipmitool hpm activate

PICMG HPM.1 Upgrade Agent 1.0.9:

Waiting firmware activation...OK
```

The front panel FRU LED’s 1 and 2 (green BMC and green payload LED) are flashing during the FW update activation! This procedure needs around 60 seconds to finalize the update.

4.4 FPGA configuration upgrade

4.4.1 Load new FPGA image

Type IPMItool HPM.1 upgrade command and select the new FPGA image.

```
[root@localhost ~]# ipmitool hpm upgrade
mic6313_fpga_standard_01_14.img

PICMG HPM.1 Upgrade Agent 1.0.9:

Validating firmware image integrity...OK
Performing preparation stage...
Services may be affected during upgrade. Do you wish to con-
tinue? (y/n): y
OK

Performing upgrade stage:

--------------------------------------------------------------
------------------
|ID  | Name            |                      Ver-
sions                                  |
|    |                 |     Active      |     Backup        |
File          |     |
|----|-------------|-----------------|-----------------|-----
------------|----|
|*  2|6313 FPGA    |   1.14 00000000 | ---.-- -------- |   1.14
00000022   |100% |
|     |Upload Time: 00:15              | Image Size:  104428
bytes                    |
--------------------------------------------------------------
------------------
(*) Component requires Payload Cold Reset

Firmware upgrade procedure successful
```

4.4.2 Activate FPGA configuration

Although the new FPGA configuration is successfully stored on the board (“deferred” version), the firmware must be activated before loading onto the FPGA chip. Perform the following two actions to activate the firmware and complete the upgrade:

4.4.2.1 HPM.1 Activate Command

Schedule FPGA loading using the HPM.1 activate command shown below.

```
[root@localhost ~]# ipmitool hpm activate

PICMG HPM.1 Upgrade Agent 1.0.9:
```

4.4.2.2 Payload Cold Reset

To activate the new FPGA image a payload cold reset is required.

```
(*) Component requires Payload Cold Reset
```

The payload reset can be performed using either of the following methods:

- For users working on the local OS (KCS), a linux “reboot”, “power off”, or “halt” operation is required.
- For users accessing the BMC through an alternate interface (LAN/IPMB), a deactivation and activation cycle is required to update the FPGA.

The front panel FRU LEDs 1 and 2 (the green BMC and green payload LEDs) should be flashing during the firmware update activation. The system should take approximately 200 seconds to finalize the update.

4.5 BIOS Upgrade

4.5.1 Load New BIOS Image

Input the IPMItool HPM.1 upgrade command and select the new BIOS image.

```
[root@localhost ~]# ipmitool hpm upgrade
mic6313_bios_V_00_20.img

PICMG HPM.1 Upgrade Agent 1.0.9:

Validating firmware image integrity...OK
Performing preparation stage...
Services may be affected during upgrade. Do you wish to con-
tinue? y/n y
OK

Performing upgrade stage:

------------------------------------------------------------
------------------
|ID  | Name           |                      Ver-
sions                              | %   |
|    |              |     Active      |     Backup       |
File          |     |
|----|--------------|-----------------|-----------------|-----
------------|----|
|*  3|6313 BIOS    |   0.20 00000000 | ---.-- -------- |   0.20
00000000   |100% |
|     |Upload Time: 12:15             | Image Size:  8,388,751
bytes                   |
------------------------------------------------------------
------------------
 (*) Component requires Payload Cold Reset

Firmware upgrade procedure successful
```

4.5.2 Activate BIOS Image

After the new BIOS image is successfully loaded (known as the “deferred” version), the image must be activated to enable booting of the new BIOS. Perform the following two actions to activate the BIOS image and complete the upgrade.

4.5.2.1 HPM.1 Activate Command

Schedule BIOS loading using the HPM.1 activate command: shown below.

```
[root@localhost ~]# ipmitool hpm activate

PICMG HPM.1 Upgrade Agent 1.0.9:
```

4.5.2.2 Payload Cold Reset

A payload cold reset is required to activate the new BIOS image.

```
(*) Component requires Payload Cold Reset
```

The payload reset can be performed using either of the following methods:

- For users working on the local OS (KCS), a linux “reboot”, “power off”, or “halt” operation is required.
- For users accessing the BMC through an alternate interface (LAN/IPMB), a deactivation and activation cycle is required to load the new BIOS image.

4.6 Verify Successful Upgrades

To verify successful updates, execute the IPMItool hpm check command.

```
[root@localhost ~]# ipmitool hpm check

PICMG HPM.1 Upgrade Agent 1.0.9:

-------Target Information-------
Device Id           : 0x74
Device Revision     : 0x81
Product Id          : 0x6313
Manufacturer Id     : 0x2839 (Advantech)


-------------------------------------------------------------
-------------
|ID  | Name        |                     Ver-
sions                        |
|    |             |     Active      |     Backup      |
Deferred   |
-------------------------------------------------------------
-------------
|   0|6313 BL      |   1.01 00000000 | ---.-- -------- | ---.-
- -------- |
|   1|6313 BMC     |   1.01 00000000 |   1.01 00000000 | ---.-
- -------- |
|*  2|6313 FPGA    |   1.14 00000000 |   1.14 00000000 | ---.-
- -------- |
|*  3|6313 BIOS    |   0.20 00000000 | ---.-- -------- | ---.-
- -------- |
-------------------------------------------------------------
-------------
(*) Component requires Payload Cold Reset
```

After a successful upgrade, the new backup version should be the previously active version (if backup versions are supported). And the new active version should be the version obtained from the upload file used.

Appendix A

Pin Assignments

This appendix describes the pin assignments.

A.1 P0 Connector

Table A.1: P0 VPX I/O							
	G	**F**	**E**	**D**	**C**	**B**	**A**
1	+12V	+12V	+12V	NC	+12V	+12V	+12V
2	+12V	+12V	+12V	NC	+12V	+12V	+12V
3	+5V	+5V	+5V	NC	+5V	+5V	+5V
4	IPMB0-B_CLK	IPMB0-B_DAT	GND	-12V_AUX	GND	SYSRESET	NVMRO
5	GAP	GA4	GND	3.3V_AUX (not used)	GND	IPMB0-A_CLK	IPMB0-A_DAT
6	GA3	GA2	GND	NC	GND	GA1	GA0
7	NC	GND	NC	NC	GND	NC	NC
8	GND	PLX_REFCLK-	PLX_REFCLK+	GND	NC	NC	GND

Note! *NC = No Connection*

 # = Active Low

A.2 P1 Connector

P1 connector is Data Plane (DP) that can Support PCIE X16 lane, default setting is 2port X8 can configure to 1port X16 or 4port X4.

Table A.2: P1 VPX I/O

	G	F	E	D	C	B	A
1		GND	PCIE_P1_TX0-	PCIE_P1_TX0+	GND	PCIE_P1_RX0-	PCIE_P1_RX0+
2	GND	PCIE_P1_TX1-	PCIE_P1_TX1+	GND	PCIE_P1_RX1-	PCIE_P1_RX1+	GND
3	+VBAT_RIO	GND	PCIE_P1_TX2-	PCIE_P1_TX2+	GND	PCIE_P1_RX2-	PCIE_P1_RX2+
4	GND	PCIE_P1_TX3-	PCIE_P1_TX3+	GND	PCIE_P1_RX3-	PCIE_P1_RX3+	GND
5	SYSEN#	GND	PCIE_P1_TX4-	PCIE_P1_TX4+	GND	PCIE_P1_RX4-	PCIE_P1_RX4+
6	GND	PCIE_P1_TX5-	PCIE_P1_TX5+	GND	PCIE_P1_RX5-	PCIE_P1_RX5+	GND
7		GND	PCIE_P1_TX6-	PCIE_P1_TX6+	GND	PCIE_P1_RX6-	PCIE_P1_RX6+
8	GND	PCIE_P1_TX7-	PCIE_P1_TX7+	GND	PCIE_P1_RX7-	PCIE_P1_RX7+	GND
9		GND	PCIE_P2_TX0-	PCIE_P2_TX0+	GND	PCIE_P2_RX0-	PCIE_P2_RX0+
10	GND	PCIE_P2_TX1-	PCIE_P2_TX1+	GND	PCIE_P2_RX1-	PCIE_P2_RX1+	GND
11		GND	PCIE_P2_TX2-	PCIE_P2_TX2+	GND	PCIE_P2_RX2-	PCIE_P2_RX2+
12	GND	PCIE_P2_TX3-	PCIE_P2_TX3+	GND	PCIE_P2_RX3-	PCIE_P2_RX3+	GND
13		GND	PCIE_P2_TX4-	PCIE_P2_TX4+	GND	PCIE_P2_RX4-	PCIE_P2_RX4+
14	GND	PCIE_P2_TX5-	PE_BP2_TX5+	GND	PCIE_P2_RX5-	PCIE_P2_RX5+	GND
15		GND	PCIE_P2_TX6-	PCIE_P2_TX6+	GND	PCIE_P2_RX6-	PCIE_P2_RX6+
16	GND	PCIE_P2_TX7-	PCIE_P2_TX7+	GND	PCIE_P2_RX7-	PCIE_P2_RX7+	GND

Note! *NC = No Connection*

 # = Active Low

SYS_CON# : (grounded: System controller) / (open : not System controller)

A.3 P2 Connector

The P2 connector supports two PCIE ports, with eight lanes per port. This can also be configured as four 4-lane ports or one 16-lane port. Six GPIO pins are reserved and can be defined by the user.

Table A.3: P2: I/O

	G	F	E	D	C	B	A
1	HDDErase_LED	GND	PCIE_P1_TX0-	PCIE_P1_TX0+	GND	PCIE_P1_RX0-	PCIE_P1_RX0+
2	GND	PCIE_P1_TX1-	PCIE_P1_TX1+	GND	PCIE_P1_RX1-	PCIE_P1_RX1+	GND
3	HDDErase_IN#	GND	PCIE_P1_TX2-	PCIE_P1_TX2+	GND	PCIE_P1_RX2-	PCIE_P1_RX2+
4	GND	PCIE_P1_TX3-	PCIE_P1_TX3+	GND	PCIE_P1_RX3-	PCIE_P1_RX3+	GND
5	GPIO5	GND	PCIE_P1_TX4-	PCIE_P1_TX4+	GND	PCIE_P1_RX4-	PCIE_P1_RX4+
6	GND	PCIE_P1_TX5-	PCIE_P1_TX5+	GND	PCIE_P1_RX5-	PCIE_P1_RX5+	GND
7	GPIO6	GND	PCIE_P1_TX6-	PCIE_P1_TX6+	GND	PCIE_P1_RX6-	PCIE_P1_RX6+
8	GND	PCIE_P1_TX7-	PCIE_P1_TX7+	GND	PCIE_P1_RX7-	PCIE_P1_RX7+	GND
9	GPIO1	GND	PCIE_P2_TX0-	PCIE_P2_TX0+	GND	PCIE_P2_RX0-	PCIE_P2_RX0+
10	GND	PCIE_P2_TX1-	PCIE_P2_TX1+	GND	PCIE_P2_RX1-	PCIE_P2_RX1+	GND
11	GPIO2	GND	PCIE_P2_TX2-	PCIE_P2_TX2+	GND	PCIE_P2_RX2-	PCIE_P2_RX2+
12	GND	PCIE_P2_TX3-	PCIE_P2_TX3+	GND	PCIE_P2_RX3-	PCIE_P2_RX3+	GND
13	GPIO3	GND	PCIE_P2_TX4-	PCIE_P2_TX4+	GND	PCIE_P2_RX4-	PCIE_P2_RX4+
14	GND	PCIE_P2_TX5-	PE_BP2_TX5+	GND	PCIE_P2_RX5-	PCIE_P2_RX5+	GND
15	GPIO4	GND	PCIE_P2_TX6-	PCIE_P2_TX6+	GND	PCIE_P2_RX6-	PCIE_P2_RX6+
16	GND	PCIE_P2_TX7-	PCIE_P2_TX7+	GND	PCIE_P2_RX7-	PCIE_P2_RX7+	GND

Note! *NC = No Connection*

 # = Active Low

A.4 P3 Connector (Reserved)

Table A.4: P3 VPX I/O								
Wafer Offset	**Row G**	**Row F**	**Row E**	**Row D**	**Row C**	**Row B**	**Row A**	
n+1		GND	Jn4-1	Jn4-3	GND	Jn4-2	Jn4-4	
N+2	GND	Jn4-5	Jn4-7	GND	Jn4-6	Jn4-8	GND	
N+3		GND	Jn4-9	Jn4-11	GND	Jn4-10	Jn4-12	
N+4	GND	Jn4-13	Jn4-15	GND	Jn4-14	Jn4-16	GND	
N+5		GND	Jn4-17	Jn4-19	GND	Jn4-18	Jn4-20	
N+6	GND	Jn4-21	Jn4-23	GND	Jn4-22	Jn4-24	GND	
N+7		GND	Jn4-25	Jn4-27	GND	Jn4-26	Jn4-28	
N+8	GND	Jn4-29	Jn4-31	GND	Jn4-30	Jn4-32	GND	P64s
N+9		GND	Jn4-33	Jn4-35	GND	Jn4-34	Jn4-36	
N+10	GND	Jn4-37	Jn4-39	GND	Jn4-38	Jn4-40	GND	
N+11		GND	Jn4-41	Jn4-43	GND	Jn4-42	Jn4-44	
N+12	GND	Jn4-45	Jn4-47	GND	Jn4-46	Jn4-48	GND	
N+13		GND	Jn4-49	Jn4-51	GND	Jn4-50	Jn4-52	
N+14	GND	Jn4-53	Jn4-55	GND	Jn4-54	Jn4-56	GND	
N+15		GND	Jn4-57	Jn4-59	GND	Jn4-58	Jn4-60	
N+16	GND	Jn4-61	Jn4-63	GND	Jn4-62	Jn4-64	GND	

Note! *NC = No Connection*

 # = Active Low

A.5 P4 Connector

The P4 connector supports an XMC card (X8d+X12d). Three GPIO pins are reserved and can be defined by the user.

Two 1G Base-T ports are provided and can be configured to two SerDes ports (optional).

Table A.5: P4 VPX I/O

	G	F	E	D	C	B	A
1	RIO_SATA_LED	GND	Jn6-A5	Jn6-B5	GND	Jn6-D5	Jn6-E5
2	GND	Jn6-A7	Jn6-B7	GND	Jn6-D7	Jn6-E7	GND
3	RIO_PRESENT#	GND	Jn6-A9	Jn6-B9	GND	Jn6-D9	Jn6-E9
4	GND	Jn6-A15	Jn6-B15	GND	Jn6-D15	Jn6-E15	GND
5	NC	GND	Jn6-A17	Jn6-B17	GND	Jn6-D17	Jn6-E17
6	GND	Jn6-A19	Jn6-B19	GND	Jn6-D19	Jn6-E19	GND
7	NC	GND	Jn6-A1	Jn6-B1	GND	Jn6-D1	Jn6-E1
8	GND	Jn6-A3	Jn6-B3	GND	Jn6-D3	Jn6-E3	GND
9	NC	GND	Jn6-A11	Jn6-B11	GND	Jn6-D11	Jn6-E11
10	GND	Jn6-A13	Jn6-B13	GND	Jn6-D13	Jn6-E13	GND
11	GPIO14	GND	SERDES2_TX-	SERDES2_TX+	GND	SERDES2_RX-	SERDES2_RX+
12	GND	SERDES1_TX-	SERDES1_TX+	GND	SERDES1_RX-	SERDES1_RX+	GND
13	GPIO15	GND	GBE2_DB-	GBE2_DB+	GND	GBE2_DA-	GBE2_DA+
14	GND	GBE2_DD-	GBE2_DD+	GND	GBE2_DC-	GBE2_DC+	GND
15	GPIO16	GND	GBE1_DB-	GBE1_DB+	GND	GBE1_DA-	GBE1_DA+
16	GND	GBE1_DD-	GBE1_DD+	GND	GBE1_DC-	GBE1_DC+	GND

Note! *NC = No Connection*

 # = Active Low

A.6 P5 Connector

The P5 connector supports two DVI ports, one VGA port, two USB 3.0 ports, three Gen 3 SATA ports, and two UART ports.

Table A.6: P5 VPX I/O

	G	F	E	D	C	B	A
1	DP2_HPD	GND	DVI2_D1-	DVI2_D1+	GND	DVI2_D2-	DVI2_D2+
2	GND	DVI2_CLK-	DVI2_CLK+	GND	DVI2_D0-	DVI2_D0+	GND
3	DP1_HPD	GND	DVI1_D1-	DVI 1_D1+	GND	DVI1_D2-	DVI1_D2+
4	GND	DVI1_CLK-	DVI1_CLK+	GND	DVI1_D0-	DVI1_D0+	GND
5	RED	GND			GND		
6	GND	USB3_5_TX+	USB3_5_Tx-	GND	USB3_5_RX-	USB3_5_RX+	GND
7	GREEN	GND	USB3_6_TX-	USB3_6_TX+	GND	USB3_6_RX-	USB3_6_RX+
8	GND	SATA4_TX-	SATA4_Tx+	GND	SATA4_RX-	SATA4_RX+	GND
9	BLUE	GND	SATA5_Tx-	SATA5_Tx+	GND	SATA5_RX-	SATA5_RX+
10	GND	DPC_CTRL_DATA	DPC_CTRL_CLK	GND	DPB_CTRL_DATA	DPB_CTRL_CLK	GND
11	H_SYNC	GND	SATA1_TX-	SATA1_TX+	GND	SATA1_RX-	SATA1_RX+
12	GND	USB4-	USB4+	GND	USB3-	USB3+	GND
13	V_SYNC	GND	COM1_DCD	COM1_RI	GND	COM1_RX	COM1_TX
14	GND	COM1_RTS	COM1_CTS	GND	COM1_DTR	COM1_DSR	GND
15	VGA_DDAT	GND	COM2_DCD	COM2_RI	GND	COM2_RX	COM2_TX
16	GND	COM2_RTS	COM2_CTS	GND	COM2_DTR	COM2_DSR	GND

Note! *NC = No Connection*

 # = Active Low

A.7 P6 Connector

The P6 connector supports two 1G Base-T ports, five USB 2.0 ports, one Gen 2 SATA port, two UART ports, one PS2 keyboard/ mouse port, one Line In/Out, and one microphone port. Four GPIO pins are reserved and can be defined by the user.

Table A.7: P6 VPX I/O

	G	F	E	D	C	B	A
1	VGA_DCLK	GND	USB6-	USB6+	GND	USB5-	USB5+
2	GND	USB8-	USB8+	GND	USB7-	USB7+	GND
3	SW2_1	GND	USB9-	USB9+	GND		
4	GND	SATA3_TX-	SATA3_TX+	GND	SATA3_RX-	SATA3_RX+	GND
5	+VBAT	GND	COM3_DCD	COM3_RI	GND	COM3_RX	COM3_TX
6	GND	COM3_RTS	COM3_CTS	GND	COM3_DTR	COM3_DSR	GND
7	RIO_GPIO7	GND	COM4_DCD	COM4_RI	GND	COM4_RX	COM4_TX
8	GND	COM4_RTS	COM4_CTS	GND	COM4_DTR	COM4_DSR	GND
9	RIO_GPIO8	GND	GBE4_DB-	GBE4_DB+	GND	GBE4_DA-	GBE4_DA+
10	GND	GBE4_DD-	GBE4_DD+	GND	GBE4_DC-	GBE4_DC+	GND
11	RIO_GPIO9	GND	GBE3_DB-	GBE3_DB+	GND	GBE3_DA-	GBE3_DA+
12	GND	GBE3_DD-	GBE3_DD+	GND	GBE3_DC-	GBE3_DC+	GND
13	RIO_GPIO10	GND	KB_CLK	KB_DAT	GND	MSC_DATA	MSC_CLK
14	GND	LINEOUT_R	LINEOUT_L	GND	RIO_GPIO5	RIO_BTN	GND
15	LINE1_JD	GND	LIN_R	LIN_L	GND	J6_MIC_JD	FRONT-JD
16	GND	AGND	A_GND	GND	MIC_R	MIC_L	GND

Note! *NC = No Connection*

 # = Active Low

A.8 Additional Connectors

Table A.8: CNSATA1 Daughter Board Connector			
1	GND	2	GND
3	SATA0_TX+	4	NC
5	SATA0_TX-	6	NC
7	GND	8	GND
9	SATA0_RX+	10	NC
11	SATA0_RX-	12	NC
13	GND	14	GND
15	GND	16	GND
17	VCC5	18	VCC3
19	VCC5	20	VCC3

Table A.9: J15 (P15) Connector						
Pin	**A**	**B**	**C**	**D**	**E**	**F**
1	PETX_P0	PETX_N0	+3.3V	PETX_P1	PETX_N1	VPWR(+5V)
2	GND	GND	NC(JRST#)	GND	GND	PRST#
3	PETX_P2	PETX_N2	+3.3V	PETX_P3	PETX_N3	VPWR(+5V)
4	GND	GND	NC(JTCK)	GND	GND	NC (MRSTO#)
5	PETX_P4	PETX_N4	+3.3V	PETX_P5	PETX_N5	VPWR(+5V)
6	GND	GND	NC(JTMS)	GND	GND	+12V
7	PETX_P6	PETX_N6	+3.3V	PETX_P7	PETX_N7	VPWR(+5V)
8	GND	GND	NC(JTDI)	GND	GND	-12V
9	NC	NC	NC	NC	NC	VPWR(+5V)
10	GND	GND	NC(JTDO)	GND	GND	GA0
11	PERX_P0	PERX_N0	NC(MBIST#)	PERX_P1	PERX_N1	VPWR(+5V)
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PERX_P2	PERX_N2	NC (+3.3V_AUX)	PERX_P3	PERX_N3	VPWR(+5V)
14	GND	GND	GA2	GND	GND	TBD_SDA
15	PERX_P4	PERX_N4	NC	PERX_P5	PERX_N5	VPWR(+5V)
16	GND	GND	NC(MVMRO)	GND	GND	TBD_SCLK
17	PERX_P6	PERX_N6	NC	PERX_P7	PERX_N7	NC
18	GND	GND	FPGAIO1	GND	GND	NC
19	CLK_100Mhz	CLK_100Mhz #	FPGAIO2	NC(WAKE#)	NC(ROOT#)	NC

Table A.10: VCN1 VGA Connector			
1	RED	9	+5V
2	GREEN	10	GND
3	BLUE	11	NC
4	NC	12	DDC_DATA
5	GND	13	HSYNC
6	GND	14	VSYNC
7	GND	15	DDC_CLK
8	GND		

Table A.11: CNCOM1 (RJ45) Connector			
1	DCD#	6	DSR#
2	SIN	7	RTS#
3	SOUT	8	CTS#
4	DTR#		
5	GND		

Table A.12: CN and CN5 USB Ports 1 and 2			
1	+5V (fused)	1	+5V (fused)
2	USBD0-	2	USBD1-
3	USBD0+	3	USBD1+
4	GND	4	GND

Table A.13: BT1 CMOS Battery			
1	BAT_VCC	2	GND

Table A.14: RJ1 LAN1 Connector			
1	LAN_0+	5	LAN_2-
2	LAN_0-	6	LAN_1-
3	LAN_1+	7	LAN_3+
4	LAN_2+	8	LAN_3-

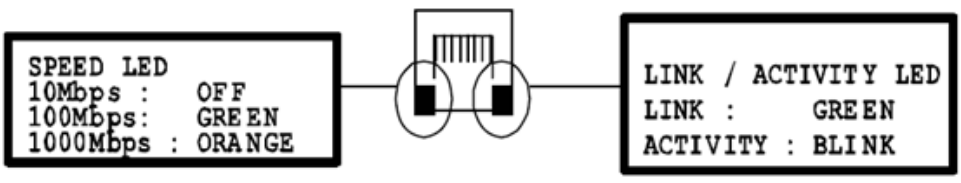
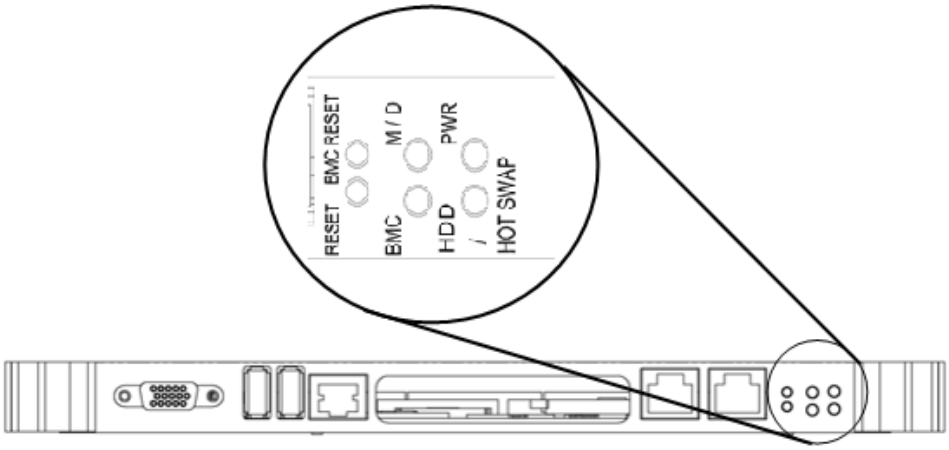


Figure A.1 RJ11 LAN indicator

A.8.1 M/D, PWR, BMC HB, and IDE/Hot-Swap LEDs



Name	Description
PWR (Green)	Indicates power status
BMC (Yellow)	Indicates BMC status (steady blinking indicates the BMC is active)
HDD/Hot Swap (Yellow/Blue)	Indicates IDE activity when yellow, and that the board is ready to be hot-swapped when blue.

Appendix B

Programming the Watchdog Timer

This appendix describes how to program the watchdog timer.

B.1 Watchdog Timer Programming Procedure

To program the watchdog timer, users must execute a program that writes a value to I/O port address 443/444 (hex) to enable/disable. This output value represents a time interval. The value range is from 01 (hex) to FF (hex), and the related time interval is 1 to 255 seconds.

Data	Time Interval
01	1 sec
02	2 sec
03	3 sec
04	4 sec
...	
3F	63 sec

After data entry, the program must refresh the watchdog timer by rewriting and setting the value of I/O port 443/443 (hex). To disable the watchdog timer, the program should read I/O port 444 (hex). The following example demonstrates how to program the watchdog timer in BASIC:

```
10 REM Watchdog timer example program
20 OUT &H443, data REM start and restart the watchdog
30 GOSUB 1000 REM Your application task #1,
40 OUT &H443, data REM reset the timer
50 GOSUB 2000 REM Your application task #2,
60 OUT &H443, data REM reset the timer
70 X=INP (&H444) REM, disable the watchdog timer
80 END
1000 REM Subroutine #1, your application task
.
1070 RETURN
2000 REM Subroutine #2, your application task
.
2090 RETURN
```

Appendix C

I/O Controller List

C.1 I/O Controller List

I/O Port	Controller
DVI to backplane	Intel Broadwell
VGA	Intel Lynx Point
Onboard flash	Intel Lynx Point
SATA	Intel Lynx Point
SATA to backplane	Intel Lynx Point
Cfast	Intel Lynx Point
USB 2.0/3.0 to front panel	Intel Lynx Point
USB 2.0/3.0 to backplane	Intel Lynx Point
Audio to backplane	Intel Lynx Point
Front panel RJ45	Intel I210
SerDes to backplane	Intel I350AM4
GBE to backplane	Intel I350AM4
UART to front panel	Lattice LCMXO2
UART to backplane	Lattice LCMXO2

Appendix D

Glossary

D.1 Glossary

ACPI	Advanced Configuration and Power Interface
BMC	Baseboard Management Controller
CPU	Central Processing Unit
CPCI	CompactPCI
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electro Magnetic Compatibility
ESD	Electro Static Discharge
FCBGA	Flip Chip BGA
HDD	Hard Disk Drive
HW	HardwareManagement
I/O	Input/Output
IC	Integrated Circuit
LED	Light Emitting Diode
LPC	Low Pin Count
LV	Low Voltage
MAC	Medium Access Control
OS	Operating System
PCB	Printed Wiring Board
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect Express
PHY	Physical layer interface
RIO	Rear Input/Output
RS232	An interface specified by the Electronic Industries Alliance
RTC	Real-Time Clock
RTM	Rear Transition Module
SBC	Single-Board Computer
SFP	Small Form-Factor Pluggable
SPD	Serial Presence Detect
SW	Software
ULV	Ultra-Low Voltage
FRU	Field-Replaceable Unit
FPGA	Field-Programmable Gate Arrays
GbE	Gigabit Ethernet
HPM	Hardware Platform Management
IOL	IPMI Over LAN
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
KCS	Keyboard Controller Style
NCSI	Network Controller Sideband Interface
NVRAM	Non-Volatile Random-Access Memory
PCH	Platform Controller Hub
PICMG	PCI Industrial Computer Manufacturers Group
PXE	Pre-Boot Execution Environment

RMCP	Remote Management Control Protocol
SDR	Sensor Data Record
SerDes	Serializer/Deserializer
SOL	Serial Over LAN
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter

Appendix E

BIOS Checkpoint

A status code is a data value used to indicate progress during the boot phase. A subset of these status codes, known commonly as checkpoints, indicates common phases of the BIOS boot process.

Checkpoints are typically output to I/O port 80h, but the Aptio 4.x core can be configured to send status codes to various locations. The Aptio 4.x core outputs checkpoints throughout the boot process to indicate the task the system is currently executing. Checkpoints are very useful to software developers and technicians for debugging problems that occur during the pre-boot process.

While performing the functions of the traditional BIOS, the Aptio 4.x core follows the firmware model described in the Intel® Platform Innovation Framework for EFI. This framework refers the following “boot phases”, which may apply to various status code and descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization
- Driver Execution Environment (DXE) – main hardware initialization
- Boot Device Selection (BDS) – system setup, pre-OS user interface and bootable device selection (CD/DVD, HDD, USB, Network, Shell)

E.1 Checkpoint Ranges/Descriptions

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 resume (PEI)
0xE9 – 0xEF	S3 resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

E.2 Standard Checkpoints

E.2.1 SEC Phase

Status Code	Description
0x00	Not used
	Progress Codes
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	Northbridge initialization before microcode loading
0x04	Southbridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	Northbridge initialization after microcode loading
0x09	Southbridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization
	SEC Error Codes
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

E.2.2 PEI Phase

Status Code	Description
	Progress Codes
0x10	PEI core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory Northbridge initialization is started
0x16	Pre-memory Northbridge initialization (Northbridge module specific)
0x17	Pre-memory Northbridge initialization (Northbridge module specific)
0x18	Pre-memory Northbridge initialization (Northbridge module specific)
0x19	Pre-memory Southbridge initialization is started
0x1A	Pre-memory Southbridge initialization (Southbridge module specific)
0x1B	Pre-memory Southbridge initialization (Southbridge module specific)
0x1C	Pre-memory Southbridge initialization (Southbridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes

0x2B	Memory initialization. Serial presence detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see the ASL status codes section below)
0x31	Memory installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application processor (AP) initialization
0x35	CPU post-memory initialization. Boot strap processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-memory Northbridge initialization is started
0x38	Post-memory Northbridge initialization (Northbridge module specific)
0x39	Post-memory Northbridge initialization (Northbridge module specific)
0x3A	Post-memory Northbridge initialization (Northbridge module specific)
0x3B	Post-memory Southbridge initialization is started
0x3C	Post-memory Southbridge initialization (Southbridge module specific)
0x3D	Post-memory Southbridge initialization (Southbridge module specific)
0x3E	Post-memory Southbridge initialization (Southbridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
	PEI Error Codes
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update has failed
0x5A	Internal CPU error
0x5B	Reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
	S3 Resume Progress Codes
0xE0	S3 resume is stared (S3 resume PPI is called by the DXE IPL)
0xE1	S3 boot script execution

0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
	S3 Resume Error Codes
0xE8	S3 resume failed
0xE9	S3 resume PPI not found
0xEA	S3 resume boot script error
0xEB	S3 OS wake error
0xEC-0xEF	Reserved for future AMI error codes
	Recovery Progress Codes
0xF0	Recovery condition triggered by firmware (auto recovery)
0xF1	Recovery condition triggered by user (forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
	Recovery Error Codes
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

E.2.3 DXE Phase

Status Code	Description
0x60	DXE core is started
0x61	NVRAM initialization
0x62	Installation of the Southbridge runtime services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	Northbridge DXE initialization is started
0x6A	Northbridge DXE SMM initialization is started
0x6B	Northbridge DXE initialization (Northbridge module specific)
0x6C	Northbridge DXE initialization (Northbridge module specific)
0x6D	Northbridge DXE initialization (Northbridge module specific)
0x6E	Northbridge DXE initialization (Northbridge module specific)
0x6F	Northbridge DXE initialization (Northbridge module specific)
0x70	Southbridge DXE initialization is started
0x71	Southbridge DXE SMM initialization is started
0x72	Southbridge devices initialization
0x73	Southbridge DXE Initialization (Southbridge module specific)
0x74	Southbridge DXE Initialization (Southbridge module specific)

0x75	Southbridge DXE Initialization (Southbridge module specific)
0x76	Southbridge DXE Initialization (Southbridge module specific)
0x77	Southbridge DXE Initialization (Southbridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot device selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI bus initialization is started
0x93	PCI bus hot plug controller initialization
0x94	PCI bus enumeration
0x95	PCI bus request resources
0x96	PCI bus assign resources
0x97	Console output devices connect
0x98	Console input devices connect
0x99	Super IO initialization
0x9A	USB initialization is started
0x9B	USB reset
0x9C	USB detect
0x9D	USB enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE reset
0xA2	IDE detect
0xA3	IDE enable
0xA4	SCSI initialization is started
0xA5	SCSI reset
0xA6	SCSI detect
0xA7	SCSI enable
0xA8	Setup verifying password
0xA9	Start of setup
0xAA	Reserved for ASL (see ASL status codes section below)
0xAB	Setup input wait
0xAC	Reserved for ASL (see ASL status codes section below)
0xAD	Ready to boot event
0xAE	Legacy boot event
0xAF	Exit boot services event
0xB0	Runtime set virtual address map begin
0xB1	Runtime set virtual address map end
0xB2	Legacy option ROM initialization
0xB3	System reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes

DXE Error Codes	
0xD0	CPU initialization error
0xD1	Northbridge initialization error
0xD2	Southbridge initialization error
0xD3	Some architectural protocols are not available
0xD4	PCI resource allocation error. Out of resources
0xD5	No space for legacy option ROM
0xD6	No console output devices are found
0xD7	No console input devices are found
0xD8	Invalid password
0xD9	Error loading boot option (LoadImage returned error)
0xDA	Boot option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

E.3 ACPI/ASL Checkpoints

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

E.4 OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post-memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

Appendix F

IPMI/PICMG Command Subset Supported by BMC

F.1 Standard IPMI Commands (v2.0)

F.1.1 IPM Device Global Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Get Device ID	20.1	App	01h	Mandatory	Yes
Cold Reset	20.2	App	02h	Optional	Yes
Warm Reset	20.3	App	03h	Optional	Yes
Get Self Test Results	20.4	App	04h	Mandatory	Yes
Manufacturing Test On	20.5	App	05h	Optional	No
Set ACPI Power State	20.6	App	06h	Optional	No
Get ACPI Power State	20.7	App	07h	Optional	No
Get Device GUID	20.8	App	08h	Optional	Yes
Broadcast 'Get Device ID'	20.9	App	01h	Optional/ Mandatory	Yes

F.1.2 BMC Watchdog Timer Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Reset Watchdog Timer	27.5	App	22h	Mandatory	Yes
Set Watchdog Timer	27.6	App	24h	Mandatory	Yes
Get Watchdog Timer	27.7	App	25h	Mandatory	Yes

F.1.3 BMC Device and Messaging Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Set BMC Global Enables	22.1	App	2Eh	Mandatory	Yes
Get BMC Global Enables	22.2	App	2Fh	Mandatory	Yes
Clear Message Flags	22.3	App	30h	Mandatory	Yes
Get Message Flags	22.4	App	31h	Mandatory	Yes
Enable Message Channel Receive	22.5	App	32h	Optional	No
Get Message	22.6	App	33h	Mandatory	Yes
Send Message	22.7	App	34h	Mandatory	Yes
Read Event Message Buffer	22.8	App	35h	Optional	Yes
Get BT Interface Capabilities	22.10	App	36h	Mandatory	No
Get System GUID	22.14	App	37h	Optional	Yes
Get Channel Authentication Capabilities	22.13	App	38h	Optional	Yes
Get Session Challenge	22.15	App	39h	Optional	Yes

Activate Session	22.17	App	3Ah	Optional	Yes
Set Session Privilege Level	22.18	App	3Bh	Optional	Yes
Close Session	22.19	App	3Ch	Optional	Yes
Get Session Info	22.20	App	3Dh	Optional	Yes
Get AuthCode	22.21	App	3Fh	Optional	No
Set Channel Access	22.22	App	40h	Optional	Yes
Get Channel Access	22.23	App	41h	Optional	Yes
Get Channel Info	22.24	App	42h	Optional	Yes
Set User Access	22.26	App	43h	Optional	Yes
Get User Access	22.27	App	44h	Optional	Yes
Set User Name	22.28	App	45h	Optional	Yes
Get User Name	22.29	App	46h	Optional	Yes
Set User Password	22.30	App	47h	Optional	Yes
Activate Payload	24.1	App	48h	-	Yes
Deactivate Payload	24.2	App	49h	-	Yes
Get Payload Activation Status	24.4	App	4Ah	-	No
Get Payload Instance Info	24.5	App	4Bh	-	No
Set User Payload Access	24.6	App	4Ch	-	Yes
Get User Payload Access	24.7	App	4Dh	-	Yes
Get Channel Payload Support	24.8	App	4Eh	-	No
Get Channel Payload Version	24.9	App	4Fh	-	No
Get Channel OEM Payload Info	24.10	App	50h	-	No
Master Write-Read	22.11	App	52h	Mandatory	Yes
Get Channel Cipher Suites	22.15	App	54h	-	Yes
Suspend/Resume Payload Encryption	24.3	App	55h	-	No
Set Channel Security Keys	22.25	App	56h	-	Yes
Get System Interface Capabilities	22.9	App	57h	-	No

F.1.4 Chassis Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Get Chassis Capabilities	28.1	Chassis	00h	Mandatory	Yes
Get Chassis Status	28.2	Chassis	01h	Optional/ Mandatory	No
Chassis Control	28.3	Chassis	02h	Optional/ Mandatory	Yes
Chassis Reset	28.4	Chassis	03h	Optional	Yes
Chassis Identify	28.5	Chassis	04h	Optional	No
Set Front Panel Button Enables	28.6	Chassis	0Ah	-	No
Set Chassis Capabilities	28.7	Chassis	05h	Optional	No
Set Power Restore Policy	28.8	Chassis	06h	Optional	Yes
Set Power Cycle Interval	28.9	Chassis	0Bh	-	No
Get System Restart Cause	28.11	Chassis	07h	Optional	No
Set System Boot Options	28.12	Chassis	08h	Optional	Yes
Get System Boot Options	28.13	Chassis	09h	Optional	Yes
Get POH Counter	28.14	Chassis	0Fh	Optional	No

F.1.5 Event Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Set Event Receiver	29.1	S/E	00h	Mandatory	Yes
Get Event Receiver	29.2	S/E	01h	Mandatory	Yes
Platform Event (a.k.a. “Event Message”)	23.3	S/E	02h	Mandatory	Yes

F.1.6 PEF and Alerting Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Get PEF Capabilities	30.1	S/E	10h	Mandatory	No
Arm PEF Postpone Timer	30.2	S/E	11h	Mandatory	No
Set PEF Configuration Parameters	30.3	S/E	12h	Mandatory	No
Get PEF Configuration Parameters	30.4	S/E	13h	Mandatory	No
Set Last Processed Event ID	30.5	S/E	14h	Mandatory	No
Get Last Processed Event ID	30.6	S/E	15h	Mandatory	No
Alert Immediate	30.7	S/E	16h	Optional	No
PET Acknowledge	30.8	S/E	17h	Optional	No

F.1.7 Sensor Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Get Device SDR Info	35.2	S/E	20h	Optional	Yes
Get Device SDR	35.3	S/E	21h	Optional	Yes
Reserve Device SDR Repository	35.4	S/E	22h	Optional	Yes
Get Sensor Reading Factors	35.5	S/E	23h	Optional	No
Set Sensor Hysteresis	35.6	S/E	24h	Optional	No
Get Sensor Hysteresis	35.7	S/E	25h	Optional	No
Set Sensor Threshold	35.8	S/E	26h	Optional	Yes
Get Sensor Threshold	35.9	S/E	27h	Optional	Yes
Set Sensor Event Enable	35.10	S/E	28h	Optional	Yes
Get Sensor Event Enable	35.11	S/E	29h	Optional	Yes
Re-arm Sensor Events	35.12	S/E	2Ah	Optional	Yes
Get Sensor Event Status	35.13	S/E	2Bh	Optional	Yes
Get Sensor Reading	35.14	S/E	2Dh	Mandatory	Yes
Set Sensor Type	35.15	S/E	2Eh	Optional	No
Get Sensor Type	35.16	S/E	2Fh	Optional	No

F.1.8 FRU Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Get FRU Inventory Area Info	34.1	Storage	10h	Mandatory	Yes
Read FRU Data	34.2	Storage	11h	Mandatory	Yes
Write FRU Data	34.3	Storage	12h	Mandatory	Yes

F.1.9 SDR Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Get SDR Repository Info	33.9	Storage	20h	Mandatory	Yes
Get SDR Repository Allocation Info	33.10	Storage	21h	Optional	No
Reserve SDR Repository	33.11	Storage	22h	Mandatory	Yes
Get SDR	33.12	Storage	23h	Mandatory	Yes
Add SDR	33.13	Storage	24h	Mandatory	No
Partial Add SDR	33.14	Storage	25h	Mandatory	No
Delete SDR	33.15	Storage	26h	Optional	No
Clear SDR Repository	33.16	Storage	27h	Mandatory	Yes
Get SDR Repository Time	33.17	Storage	28h	Optional/ Mandatory	Yes

Set SDR Repository Time	33.18	Storage	29h	Optional/ Mandatory	Yes
Enter SDR Repository Update Mode	33.19	Storage	2Ah	Optional	No
Exit SDR Repository Update Mode	33.20	Storage	2Bh	Mandatory	No
Run Initialization Agent	33.21	Storage	2Ch	Optional	No

F.1.10 SEL Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Get SEL Info	31.2	Storage	40h	Mandatory	Yes
Get SEL Allocation Info	31.3	Storage	41h	Optional	No
Reserve SEL	31.4	Storage	42h	Optional	Yes
Get SEL Entry	31.5	Storage	43h	Mandatory	Yes
Add SEL Entry	31.6	Storage	44h	Mandatory	Yes
Partial Add SEL Entry	31.7	Storage	45h	Mandatory	No
Delete SEL Entry	31.8	Storage	46h	Optional	No
Clear SEL	31.9	Storage	47h	Mandatory	Yes
Get SEL Time	31.10	Storage	48h	Mandatory	Yes
Set SEL Time	31.11	Storage	49h	Mandatory	Yes
Get Auxiliary Log Status	31.12	Storage	5Ah	Optional	No
Set Auxiliary Log Status	31.13	Storage	5Bh	Optional	No

F.1.11 LAN Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Set LAN Configuration Parameters	23.1	Trans-port	01h	Optional/ Mandatory	Yes
Get LAN Configuration Parameters	23.2	Trans-port	02h	Optional/ Mandatory	Yes
Suspend BMC ARPs	23.3	Trans-port	03h	Optional/ Mandatory	No
Get IP/UDP/RMCP Statis-tics	23.4	Trans-port	04h	Optional	No

F.1.12 Serial/Modem Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Set Serial/Modem Configuration	25.1	Transport	10h	Optional/ Mandatory	No
Get Serial/Modem Configuration	25.2	Transport	11h	Optional/ Mandatory	No

Set Serial/Modem Mux	25.3	Transport	12h	Optional	No
Get TAP Response Codes	25.4	Transport	13h	Optional	No
Set PPP UDP Proxy Transmit Data	25.5	Transport	14h	Optional	No
Get PPP UDP Proxy Transmit Data	25.6	Transport	15h	Optional	No
Send PPP UDP Proxy Packet	25.7	Transport	16h	Optional	No
Get PPP UDP Proxy Receive Data	25.8	Transport	17h	Optional	No
Serial/Modem Connection Active	25.9	Transport	18h	Optional/ Mandatory	No
Callback	25.10	Transport	19h	Optional	No
Set User Callback Options	25.11	Transport	1Ah	Optional	No
Get User Callback Options	25.12	Transport	1Bh	Optional	No
SOL Activating	26.1	Transport	20h	-	Yes
Set SOL Configuration Parameters	26.2	Transport	21h	-	Yes
Get SOL Configuration Parameters	26.3	Transport	22h	-	Yes

F.1.13 Bridge Management Commands (ICMB)

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Get Bridge State	[ICMB]	Bridge	00h	Optional/ Mandatory	No
Set Bridge State	[ICMB]	Bridge	01h	Optional/ Mandatory	No
Get ICMB Address	[ICMB]	Bridge	02h	Optional/ Mandatory	No
Set ICMB Address	[ICMB]	Bridge	03h	Optional/ Mandatory	No
Set Bridge Proxy Address	[ICMB]	Bridge	04h	Optional/ Mandatory	No
Get Bridge Statistics	[ICMB]	Bridge	05h	Optional/ Mandatory	No
Get ICMB Capabilities	[ICMB]	Bridge	06h	Optional/ Mandatory	No
Clear Bridge Statistics	[ICMB]	Bridge	08h	Optional/ Mandatory	No
Get Bridge Proxy Address	[ICMB]	Bridge	09h	Optional/ Mandatory	No
Get ICMB Connector Info	[ICMB]	Bridge	0Ah	Optional/ Mandatory	No
Get ICMB Connection ID	[ICMB]	Bridge	0Bh	Optional/ Mandatory	No
Send ICMB Connection ID	[ICMB]	Bridge	0Ch	Optional/ Mandatory	No

F.1.14 Discovery Commands (ICMB)

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Prepare For Discovery	[ICMB]	Bridge	10h	Optional/ Mandatory	No
Get Addresses	[ICMB]	Bridge	11h	Optional/ Mandatory	No
Set Discovered	[ICMB]	Bridge	12h	Optional/ Mandatory	No
Get Chassis Device ID	[ICMB]	Bridge	13h	Optional/ Mandatory	No
Set Chassis Device ID	[ICMB]	Bridge	14h	Optional/ Mandatory	No

F.1.15 Bridging Commands (ICMB)

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Bridge Request	[ICMB]	Bridge	20h	Optional/ Mandatory	No
Bridge Message	[ICMB]	Bridge	21h	Optional/ Mandatory	No

F.1.16 Event Commands (ICMB)

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Get Event Count	[ICMB]	Bridge	30h	Optional/ Mandatory	No
Set Event Destination	[ICMB]	Bridge	31h	Optional/ Mandatory	No
Set Event Reception State	[ICMB]	Bridge	32h	Optional/ Mandatory	No
Send ICMB Event Message	[ICMB]	Bridge	33h	Optional/ Mandatory	No
Get Event Destination	[ICMB]	Bridge	34h	Optional/ Mandatory	No
Get Event Reception State	[ICMB]	Bridge	35h	Optional/ Mandatory	No

F.1.17 OEM Commands for Bridge NetFn

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
OEM Commands	[ICMB]	Bridge	C0h-FEh	Optional/ Mandatory	No

F.1.18 Other Bridge Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Error Report	[ICMB]	Bridge	FFh	Optional/ Mandatory	No

F.2 PICMG IPMI Commands

F.2.1 AdvancedTCA (PICMG 3.0 R3.0 Base Specification)

Command	PICMG 3.0 Table	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Get PICMG Properties	3-11	PICMG	00h	-	Yes
Get Address Info	3-10	PICMG	01h	-	No
Get Shelf Address Info	3-16	PICMG	02h	-	No
Set Shelf Address Info	3-17	PICMG	03h	-	No
FRU Control	3-27	PICMG	04h	-	Yes
Get FRU LED Properties	3-29	PICMG	05h	-	Yes
Get LED Color Capabilities	3-30	PICMG	06h	-	Yes
Set FRU LED State	3-31	PICMG	07h	-	Yes
Get FRU LED State	3-32	PICMG	08h	-	Yes
Set IPMB State	3-70	PICMG	09h	-	No
Set FRU Activation Policy	3-20	PICMG	0Ah	-	No
Get FRU Activation Policy	3-21	PICMG	0Bh	-	No
Set FRU Activation	3-19	PICMG	0Ch	-	No
Get Device Locator Record ID	3-39	PICMG	0Dh	-	Yes
Set Port State	3-59	PICMG	0Eh	-	No
Get Port State	3-60	PICMG	0Fh	-	No
Compute Power Properties	3-82	PICMG	10h	-	No
Set Power Level	3-84	PICMG	11h	-	No
Get Power Level	3-83	PICMG	12h	-	No
Renegotiate Power	3-91	PICMG	13h	-	No
Get Fan Speed Properties	3-86	PICMG	14h	-	No
Set Fan Level	3-88	PICMG	15h	-	No
Get Fan Level	3-87	PICMG	16h	-	No
Bused Resource	3-62	PICMG	17h	-	No
Get IPMB Link Info	3-68	PICMG	18h	-	No
Get Shelf Manager IPMB Address	3-38	PICMG	1Bh	-	No
Set Fan Policy	3-89	PICMG	1Ch	-	No
Get Fan Policy	3-90	PICMG	1Dh	-	No
FRU Control Capabilities	3-26	PICMG	1Eh	-	Yes
FRU Inventory Device Lock Control	3-42	PICMG	1Fh	-	No
FRU Inventory Device Write	3-43	PICMG	20h	-	No

Get Shelf Manager IP-Addresses	3-36	PICMG	21h	-	No
Get Shelf Power Allocation	3-85	PICMG	22h	-	No
Get Telco Alarm Capability	3-93	PICMG	29h	-	No
Set Telco Alarm State	3-94	PICMG	2Ah	-	No
Get Telco Alarm State	3-95	PICMG	2Bh	-	No
Get Telco Alarm Location	3-96	PICMG	39h	-	No
Set FRU Extracted	3-25	PICMG	3Ah	-	No

F.2.2 HPM.1 (R1.0)

Command	HPM.1 Table	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Get target upgrade capabilities	3-3	PICMG	2Eh	-	Yes
Get component properties	3-5	PICMG	2Fh	-	Yes
Abort Firmware Upgrade	3-15	PICMG	30h	-	Yes
Initiate upgrade action	3-8	PICMG	31h	-	Yes
Upload firmware block	3-9	PICMG	32h	-	Yes
Finish firmware upload	3-10	PICMG	33h	-	Yes
Get upgrade status	3-2	PICMG	34h	-	Yes
Activate firmware	3-11	PICMG	35h	-	Yes
Query Self-test Results	3-12	PICMG	36h	-	Yes
Query Rollback status	3-13	PICMG	37h	-	Yes
Initiate Manual Rollback	3-14	PICMG	38h	-	Yes

F.3 OEM/Group IPMI Commands

F.3.1 Advantech OEM Commands

Command	NetFn	CMD	IPMI BMC Req.	Advantech BMC Support
Store Configuration Settings	OEM/ Group	40h	-	Yes
Read Configuration Settings	OEM/ Group	41h	-	Yes
Read Port 80	OEM/ Group	80h	-	Yes
Clear NVRAM Data	OEM/ Group	81h	-	Yes
Read MAC Address	OEM/ Group	E2h	-	Yes
Load Default Configuration	OEM/ Group	F2h	-	Yes

Appendix G

Drivers and Tools

G.1 OpenIPMI

The OpenIPMI project provides an IPMI kernel driver that is available in most Linux distributions.

The Open IPMI Linux device driver is designed as a fully functional IPMI device driver with the following features:

- Allows multiple users
- Allows multiple interfaces
- Allows both kernel and userland things to use the interface
- Fully supports the watchdog timer
- Functions like an IPMI driver - tracks outgoing messages, matches responses automatically, and automatically fetches events and received messages
- Supports interrupts
- Offers backwards-compatibility modules for supporting the Radisys IPMI driver and Intel IMB driver
- Is modular, users do not need the standard userland interface or watchdog
- Supports generating an event on a panic

Source: OpenIPMI Page (http://openipmi.sourceforge.net/)

Additional information regarding the IPMI driver can be found on the OpenIPMI Project page at http://openipmi.sourceforge.net/

The KCS register interfaces are located at 0xCA2 /0xCA3 and are used by the OpenIPMI driver as default.

G.2 IPMItool

The IPMItool provides an easy-to-use set of functions and commands for accessing the BMC via the KCS interface from within the MIC-6314 OS or via Ethernet through NC-SI from an external device. The IPMItool also allows bridged IPMI commands to access the BMC if the carrier manager provides an IPMI-over-LAN interface. See Chapters 3 and 4 for more details regarding different access methods and IPMItool calls.

The IPMITool source code can be downloaded from the official project page at http://ipmitool.sourceforge.net.

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